ACE34LA04A

Memory Module TS with 4 Kbit SPD EEPROM

Description

The ACE34LA04A is targeted for DDR4 Dual Inline Memory Modules (DIMM) in servers, laptops, desktops and other industrial applications. It is compliant with the JEDEC specification TSE2004B2, which defines memory module Temperature Sensor (TS) requirements for use in DRAM DIMMs with Serial Presence Detect (SPD), in which all the information concerning the DRAM module configuration such as its access speed, its size, its organization.

The SPD is a 4-Kbit serial EEPROM (EE) in ACE34LA04A, which is organized as two pages of 256 bytes each, or 512 bytes of total memory. Each page is comprised of two 128-byte blocks. The SPD is able to selectively lock the data in any or all of the four 128-byte blocks. Individually locking a 128-byte block may be accomplished using a software Write Protection mechanism in conjunction with a high input voltage V_{HV} on input A0. By sending the device a specific SMBus sequence, each block may be protected from writes until the Write Protection is electrically reversed using a separate SMBus sequence which also requires V_{HV} on input A0. Write Protection for all four blocks is cleared simultaneously, and Write Protection may be reasserted after being cleared.

The TS has a programmable 9-12 bit Analog-to-Digital Converter (ADC) which monitors and digitizes the temperature to a resolution of up to 0.0625 °C. The default resolution is 0.25°C/LSB (10-bit), and typical accuracies over this temperature followed the B-Grade, ranges are:

± 0.5°C (75 °C to 95 °C)

± 1 °C (40 °C to 125 °C)

± 2 °C (–40 °C to 125 °C)

The TS has user-programmable registers that provide the capabilities for DIMM temperature-sensing applications. The open drain event output pin is active when the monitoring temperature exceeds a programmable limit, or it falls above or below an alarm window. The user has the option to set the event output as a critical temperature output. This pin can be configured to operate in either a comparator mode for thermostat operation or in interrupt mode. The user also has the option to set temperature hysteresis and lock configuration via lock bit.

The ACE34LA04A can interface to 2-wire buses with a maximum of 1 MHz transfer rate which have multiple devices on a shared bus, and each device has its own unique address on this bus. The device can achieve substantial power savings by using the software-programmed shutdown mode.

Features

- Single Supply Voltage:
  1.7V ~ 3.6V(EEPROM)
  2.2V ~ 3.6V(TS)
- Fully Compliant with JEDEC TSE2004B2 Specifications
- Operating Temperature Range: -40°C ~ 125°C
- RoHS Compliant, Halogen-free
- Packaging: UDFN8, JEDEC MO-229, W2030D Compliant
- Application: DDR4 DIMM Modules Servers, Desktops, PC, etc. Industrial Applications

Temperature Sensor

- Temperature Sensor Resolution:
  Programmable (9~12 bits)
  0.25°C (Typ)/LSB - (10-bit) default
- Temperature Sensor Accuracy (max):
  ± 1°C (75°C ~ 95°C)
  ± 2°C (40°C ~ 125°C)
  ± 3°C (–40°C ~ 125°C)
- Temperature Hysteresis: Selectable 0, 1.5, 3, 6.0°C Set Point
- ADC Conversion Time (max):
  500 mS (12-bit)
  250 mS (11-bit)
  125 mS (10-bit) (default)
  65 mS (9-bit)
- Software Programmable Shutdown Mode
- Supply Current (max):
  1mA(TS Active)
  100uA(TS Shutdown)

SPD EEPROM

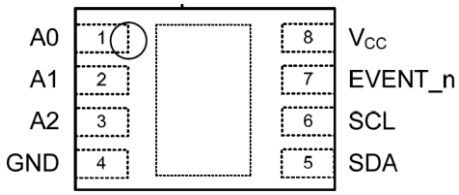
- 4-Kbit Serial Presence Detect EEPROM
- Memory Array: 4 Kbits Organized as two Page of 256 Bytes Each Page is Composed of two 128-byte Blocks
- Write Protection: Software Data Protection for Each Block
- Write Cycle:
  Byte Write within 3 mS
  Page Write (up to 16 bytes) within 3 Ms
- Random Read and Sequential Read Modes
- Automatic Address Incrementing
- High-reliability:
  Endurance: More than 1 Million Write Cycles
  Data Retention: 100 Years

Two-wire Bus

- Compatible with SMBus Serial Interface: Up to 1 MHz Transfer Rate
- Support SMBus Timeout 25mS~35mS
- Schmitt Trigger, Filtered Inputs for Noise Suppression

Packaging Type

UDFN8



Pin Configurations

Pin No	Pin Name	Type	Functions
1	A0	I	Address Inputs
2	A1	I	Address Inputs
3	A2	I	Address Inputs
4	GND	P	GND
5	SDA	I/O	Serial Data
6	SCL	I	Serial Clock Input
7	EVENT_n	O	Event Output
8	V_{CC}	P	Power Supply
	HPAD	Heat Paddle	GND(1)

Note:

(1). The ACE34LA04A has a heat paddle, which is typically connected to the application ground plane. The heat paddle is not connecting any pin in the device.

Ordering Information

ACE34LA04A XXX + X H

- Halogen - free
- U: Tube
  T: Tape and Reel
- Pb - free
- UDF: UDFN8

Pin Description

A0, A1, A2

These input signals are used to set the Logical Serial Address (LSA) that is compared to the three least significant bits (b3, b2, b1) of the 7-bit Slave Address, and must be tied to V_{CC} or GND. For details please refer to LSA Encoding.

The A0 input is also used to detect the V_{HV} voltage when decoding a SWPn or CWP instruction. When decoding the RPSn, SPAn or RPA instruction, then the A0 input don't detect the V_{HV} voltage.

For details please refer to Device Select Code (DSC).

SDA

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-ORed with other open drain or open collector signals on the bus. A pull up resistor must be connected from SDA to the most positive V_{CC} in the 2-wire bus chain. Figure 1. indicates how the value of the pull-up resistor can be calculated.

SCL

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor can be connected from SCL to V_{CC}. Figure 1. indicates how the value of the pull-up resistor can be calculated. In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

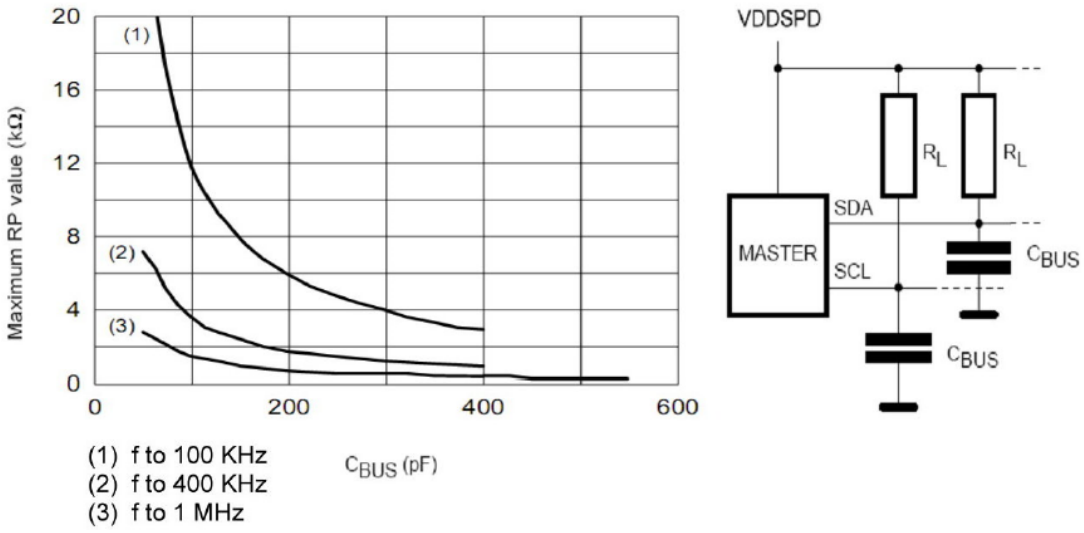


Figure 1. Maximum R_L Value VS Bus Capacitance (C_{BUS}) for 2-Wire Bus

EVENT_n

The EVENT_n pin is an open drain output that requires a pull-up resistor connect to V_{CC} on the system motherboard or integrated into the master controller. EVENT_n has three operating modes, depending on configuration settings and any current out-of-limit conditions. These modes are Interrupt, Comparator, or TCRIT Only.

In Interrupt Mode the EVENT_n pin will remain asserted until it is released by writing a '1' to the "Clear Event" bit in the configuration Register. The value to write is independent of the EVENT_n polarity bit.

In Comparator Mode the EVENT_n pin will clear itself when the error condition that caused the pin to be asserted is removed. When the temperature is compared against the TCRIT limit, then this mode is always used.

Finally, in the TCRIT Only Mode the EVENT_n pin will only be asserted if the measured temperature exceeds the TCRIT Limit. Once the pin has been asserted, it will remain asserted until the temperature drops below the TCRIT Limit minus the TCRIT hysteresis. Figure 2. illustrates the operation of the different modes over time and temperature.

Systems that use the active high mode for EVENT_n must be wired point to point between the ACE34LA04A and the sensing controller. Wire-OR configurations should not be used with active high EVENT_n since any device pulling the EVENT_n signal low will mask the other devices on the bus. Also note that the normal state of EVENT_n in active high mode is a '0', which will constantly draw power through the pull-up resistor.

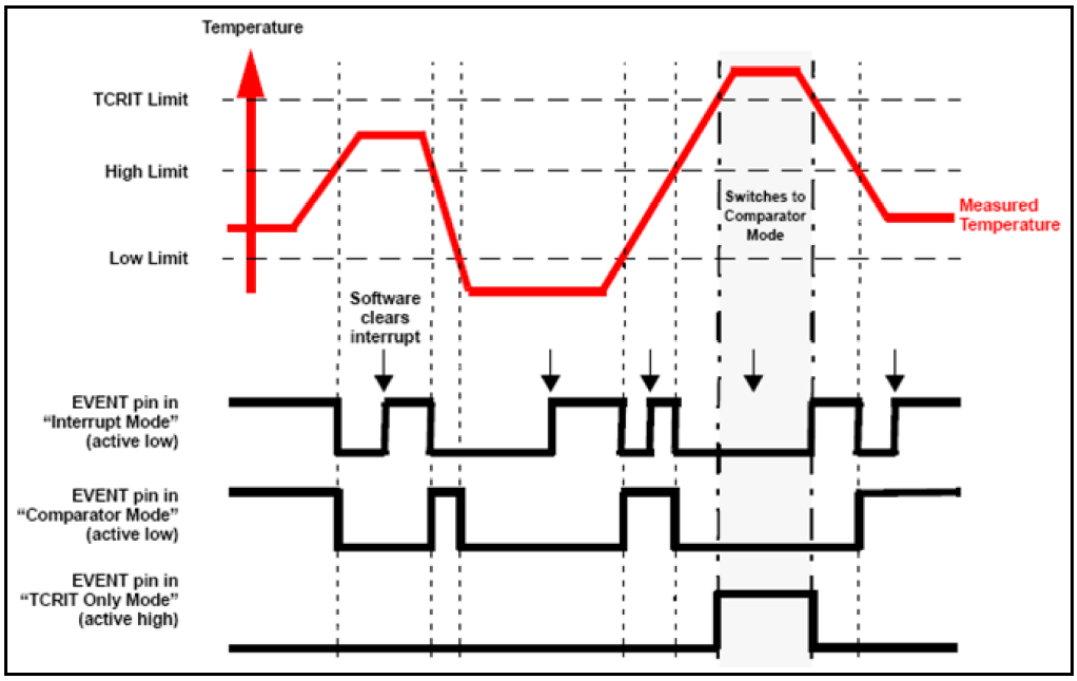
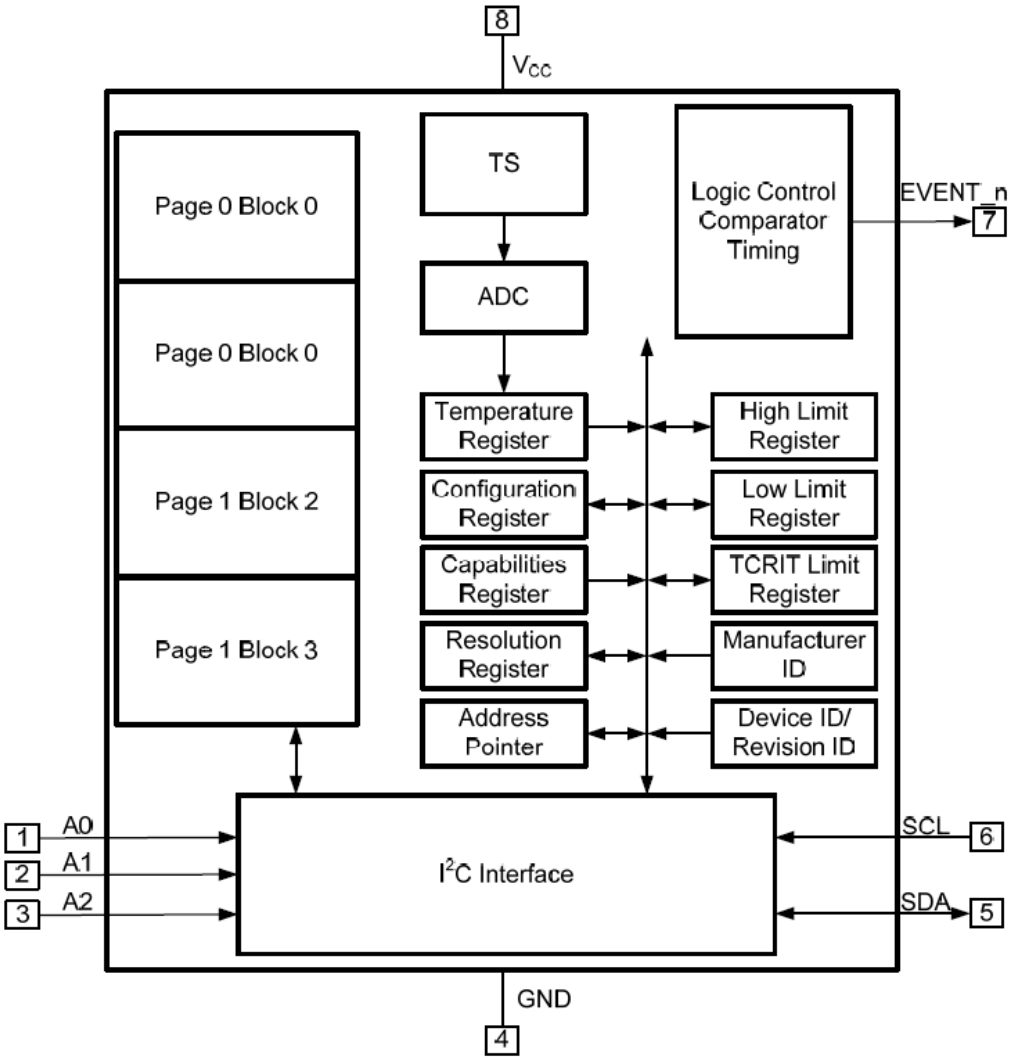


Figure 2. EVENT_n Pin Mode Functionality

HPAD

The Heat Paddle which is typically connected to the application ground plane. The heat paddle is not connecting any pin inside the device.

Block Diagram



Serial Communication

The ACE34LA04A has a simple 2-wire I^2C-compatible serial interface. User can access both the 4-Kbit SPD EEPROM and the temperature register at any time. Via the serial interface, speeds can up to 1 MHz. The device behaves as a slave device in the 2-wire bus, with all operations synchronized by the SCL. Access operations are initiated by a START condition, generated from the bus master. The START condition is followed by a Device Select Code and R/W bit (as described in Table 2), terminated by an acknowledge bit. The ACE34LA04A device is selected when decoding the correct device select byte. The device select byte is comprised of 4-bit Device Type Identifier (DTI) and 3-bit LSA.

For the operation of ACE34LA04A, when writing data to the memory or TS register, the device inserts an acknowledge bit during the 9^{th} clock cycle, following the bus master's 8-bit transmission, when data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by the bus master generated STOP condition after an Acknowledge (ACK) for Write and after a No Acknowledge (NACK) for Read. The data transfers is Most Significant Byte (MSB) first of command, address and data.

Clock stretching is not supported by the device. Violations of the command protocol result in unpredictable operation.

LSA Encoding

Table 1. 2-Wire Bus Addressing Modes

Logical Serial Address (LSA)	A2	A1	A0
000	0	0	0
001	0	0	1
010	0	1	0
011	0	1	1
100	1	0	0
101	1	0	1
110	1	1	0
111	1	1	1

Note: 0 = GND, 1 = V_{CC}

The LSA Encoding sees Table 1. When protection commands SWPn, CWP, RPSn, or page address commands SPAn and RPA is present, do not use the LSA, therefore all devices on the bus will act on these commands simultaneously. Since it is impossible to determine which device is responding to RPSn or RPA commands, for example, these functions are primarily used for external device programmers rather than in system applications.

DTI Code

The JEDEC demand TS and EEPROM each have their own unique address, which ensures that there are no compatibility or data translation issues. This is due to the fact that each of the devices has their own 4-bit DTI code and 3-bit LSA. This enables the EEPROM and TS to provide their own individual data via their unique addresses and still not interfere with each other's operation in any way.

The DTI codes are:

'0011' for the TS, and '1010' for the EEPROM memory array, and '0110' to access the software Write Protection settings and page address, and Others are forbidden.

Device Select Code

Table 2. Device Select Code

Function	Abbr	DTI[1]				LSA[2,4]			R_W	A0 Pin[3]
		b7	b6	b5	b4	b3	b2	b1	b0	
Read Temperature Registers	RTR	0	0	1	1	A2	A1	A0	1	0 or 1
Write Temperature Registers	WTR								0	
Read EE Memory	RSPD	1	0	1	0	A2	A1	A0	1	0 or 1
Write EE Memory	WSPD								0	
Set Write Protection, Block 0	SWP0	0	1	1	0	0	0	1	0	V_{HV}
Set Write Protection, Block 1	SWP1					1	0	0	0	V_{HV}
Set Write Protection, Block 2	SWP2					1	0	1	0	V_{HV}
Set Write Protection, Block 3	SWP3					0	0	0	0	V_{HV}
Clear All Write Protection	CWP					0	1	1	0	V_{HV}
Read Protection Status, Block 0	RPS0					0	0	1	1	0,1 or V_{HV}
Read Protection Status, Block 1	RPS1					1	0	0	1	0,1 or V_{HV}
Read Protection Status, Block 2	RPS2					1	0	1	1	0,1 or V_{HV}

Function	Abbr	DTI[1]				LSA[2,4]			R_W	A0 Pin[3]
		b7	b6	b5	b4	b3	b2	b1	b0	
Read Protection Status, Block 3	RPS3	0	1	1	0	0	0	0	1	0,1 or V_{HV}
Set Page Address to 0[5,7]	SPA0					1	1	0	0	0,1 or V_{HV}
Set Page Address to 1[5,7]	SPA1					1	1	1	0	0,1 or V_{HV}
Read Page Address[6]	RPA					1	1	0	1	0,1 or V_{HV}
Reserved						All Other Encodings				

Note:

1. The most significant bit, b7, is sent first.
2. LSA are generated by the combination of inputs on the A2 A1 A0 pins.
3. A0 pin is driven to 0 = GND, 1 = V_{CC}, or V_{HV}.
4. For backward compatibility with previous devices, the order of block select bits (b3 and b1) is not a simple binary encoding of the block number.
5. Set EE page address to 0 selects the lower 256 bytes of EEPROM, setting to 1 selects the upper 256 bytes of EEPROM. Subsequent Read EE or Write EE commands operate on the selected EE page.
6. Reading the EE page address results in ACK when the current page is 0 and NACK when the current page is 1.
7. No delay is required after switching pages via the SPAn commands before accessing the device.

The 8th bit is the Read/Write bit (R/W). This bit is set to 1 for Read and 0 for Write operations. For EEPROM or TS register access, if a match occurs on the Device Select Code, the corresponding device gives an acknowledgment on SDA during the 9th bit time, and if the device does not match the Device Select Code, it deselects itself from the bus, and goes into Standby Mode. The I^2C Bus operating modes are detailed in Table 3.

Table 3. I^2C Bus Operating Modes

Mode	R/W Bit	Bytes	Initial Sequence
EE Current Address Read	1	1	START, Device Select, R/W = 1
EE Random Address Read	0	1	START, Device Select, R/W = 0, Address
	1		RESTART, Device Select, R/W = 1
EE Sequential Read	1	1	Similar to Current or Random Address Read
EE Byte Write	0	1	START, Device Select, R/W = 0, data, STOP
EE Page Write	0	≤16	START, Device Select, R/W = 0, data, STOP
TS Write	0	2	START, Device Select, R/W=0, pointer, data, STOP
TS Read	1	2	START, Device Select, R/W=1, pointer, data, STOP

For the SWPn, CWP, RPSn, SPAn, RPA command, during the 9th bit time, device gives an ACK or NACK (see Write Protection).

Wave Condition

Clock and Data Transition

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 3). Data changes during SCL high periods will indicate a START or STOP condition as defined below.

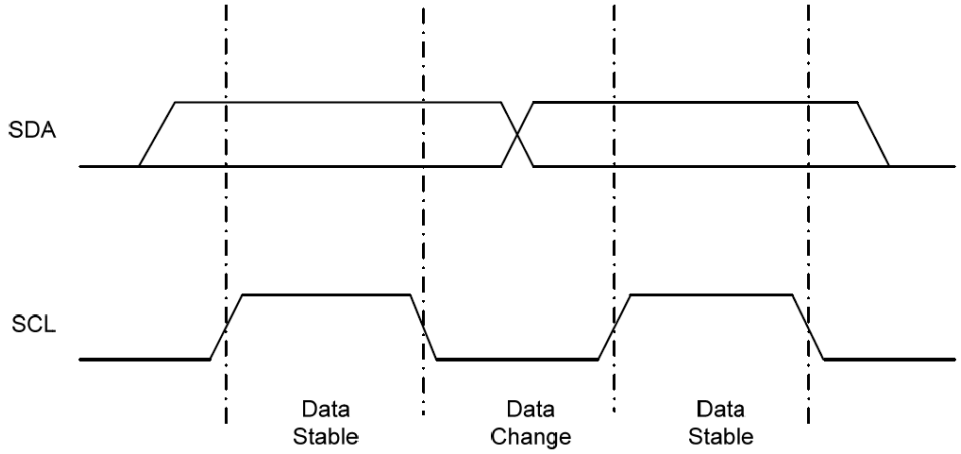


Figure 3. Data Validity

START

A high-to-low transition of SDA with SCL high is a START condition which must precede any other command (see Figure 4).

STOP

A low-to-high transition of SDA with SCL high is a STOP condition. After a read sequence, the STOP command will place the EEPROM in a standby power mode (see Figure 4).

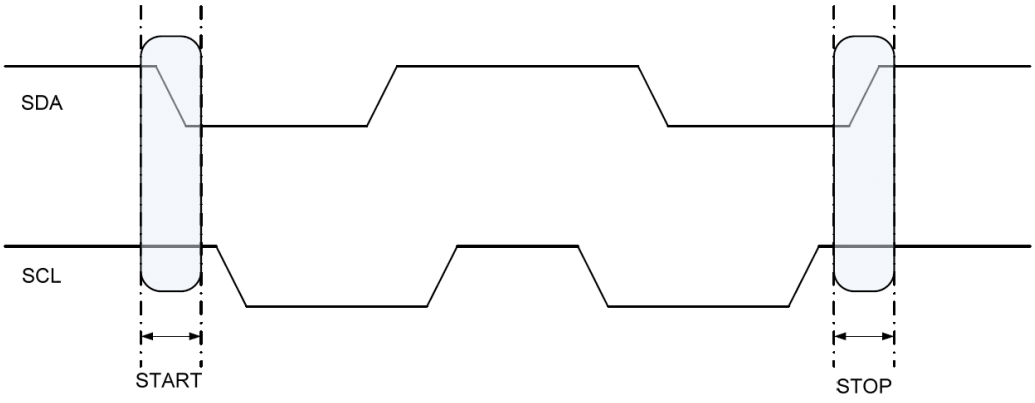


Figure 4. START and STOP Definition

Acknowledge

All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a '0' to acknowledge that it has received each word. This happens during the 9th clock cycle (see Figure 5).

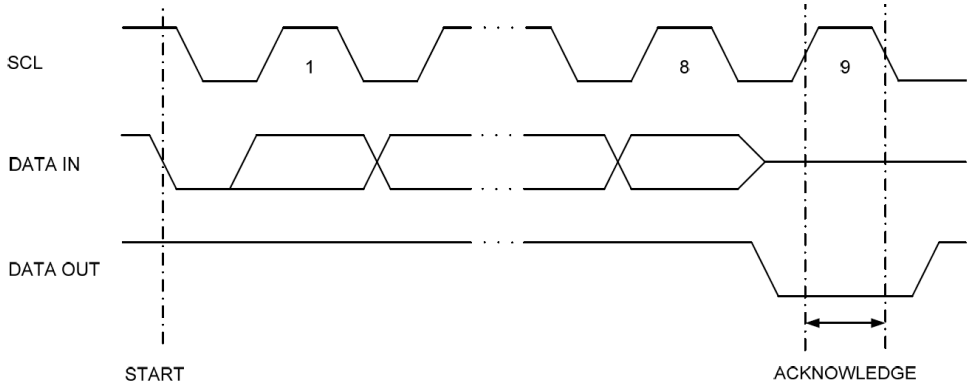


Figure 5. Output Acknowledge

SMBus Timeout

The ACE34LA04A supports the SMBus timeout feature. If the bus master holds SCL low for more than $t_{TIMEOUT\ (max)}$, the ACE34LA04A resets itself and releases the bus (see Figure 6).

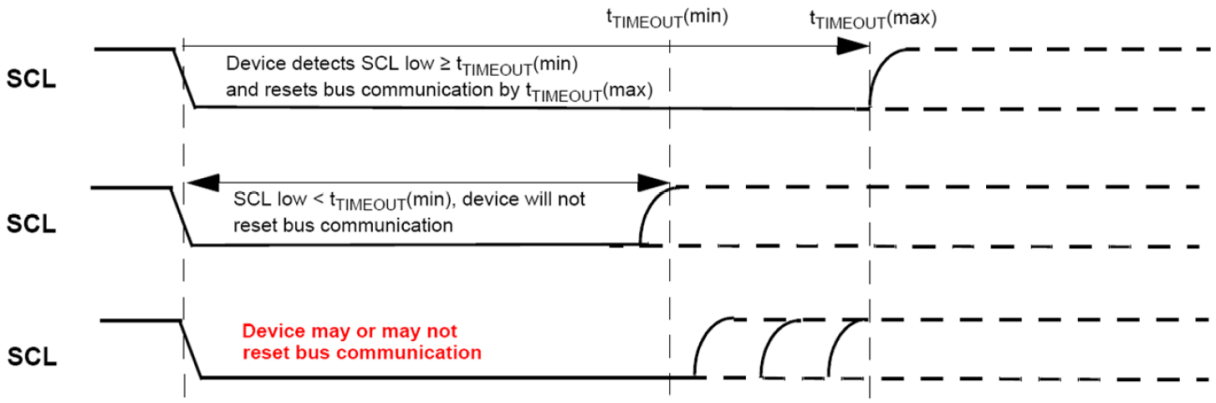


Figure 6. Timeout Feature

Internal Device Reset

In order to prevent inadvertent operations during power up, a Power on Reset (POR) circuit is included. On cold power on, V_{CC} must rise monotonically between V_{PON} and $V_{CC\ (min)}$ without ring back to ensure proper startup. Once V_{CC} has passed the V_{PON} threshold, the device is reset.

Prior to selecting the memory and issuing instructions, a valid and stable V_{CC} voltage must be applied, and no command may be issued to the device for t_{INIT}. The supply voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal Write Cycle (t_W).

At power down (phase during which V_{CC} decreases continuously), as soon as V_{CC} drops from the normal operating voltage below the minimum operating voltage, the device stops responding to commands.
On warm power cycling, V_{CC} must remain below V_{POFF} for t_{POFF}, and must meet cold power on reset timing when restoring power (see Figure 7). The ACE34LA04A delivered with all bits in the EEPROM memory array set to '1', it means that each byte is 0xFF for Read when the first used.

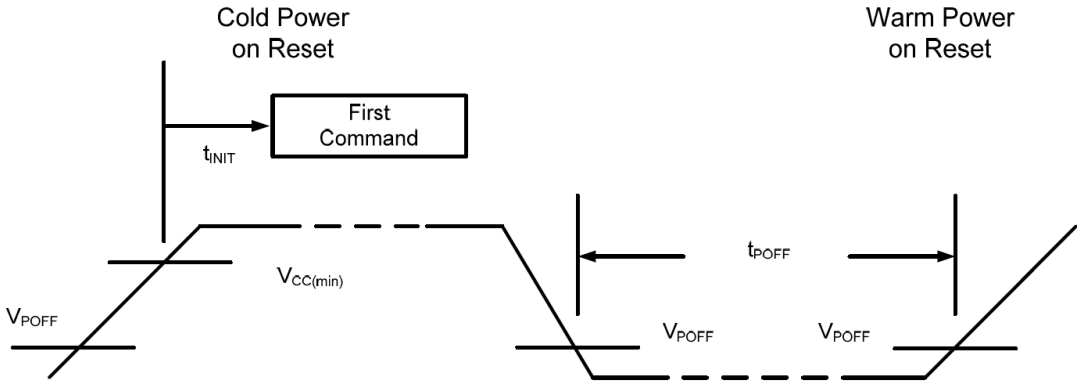


Figure 7. V_{CC} Ramp Up and Ramp Down

EEPROM Functional Description

Write Operations

Following a START condition, the bus master sends a Device Select Code with the R/W bit reset to 0. The device acknowledges this, and waits for an Address byte. The device responds to the Address byte with an ACK bit, and then waits for the Data byte.

When the bus master generates a STOP condition immediately after the ACK bit (in the 10^{th} bit time slot), either at the end of a Byte Write or a Page Write, the internal memory Write Cycle is triggered. A STOP condition at any other time slot does not trigger the internal Write Cycle.

During the internal Write Cycle, SDA and SCL are ignored by the EEPROM, and the EEPROM device does not respond to any request, but access to the TS portion of the device is permitted during this period. The device has an internal address counter which is incremented each time a byte is written. If a Write operation is performed to a protected block, the internal address counter is not incremented.

Byte Write

After the Device Select Code and the Address byte, the bus master sends one Data byte. If the addressed location is write protected, the device replies to the Data byte with NACK, and the location is not modified, and if the addressed location is not write-protected, the device replies with ACK. After the byte is transferred, the internal byte address counter is incremented unless the block is write-protected. The bus master terminates the transfer by generating a STOP condition, as shown in Figure 8.

If the addressed location is write-protected, the device replies to the Data byte with NACK, and the location is not modified.

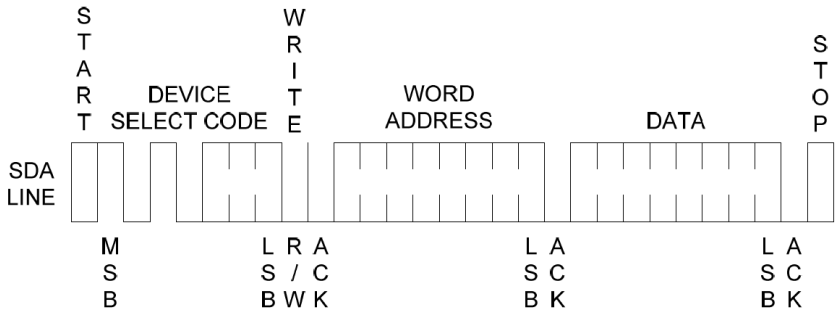


Figure 8. Byte Write

Page Write

The Page Write mode allows up to 16 bytes to be written in a single Write Cycle, provided that they are all located in the same page in the memory: that is, the most significant 4-bit memory address bits are the same. If more bytes are sent than will fit up to the end of the page, a condition known as 'roll-over' occurs. This should be avoided, as data starts to be over-written in an implementation dependent fashion.

The bus master sends from 1 to 16 bytes of Data, each of which is acknowledged by the device. If the addressed location is write-protected, the device replies to the Data byte with NACK and the locations are not modified.

After each byte is transferred, the internal byte address counter is incremented unless the block is write-protected. The transfer is terminated by the bus master generating a STOP condition, as shown in Figure 9.

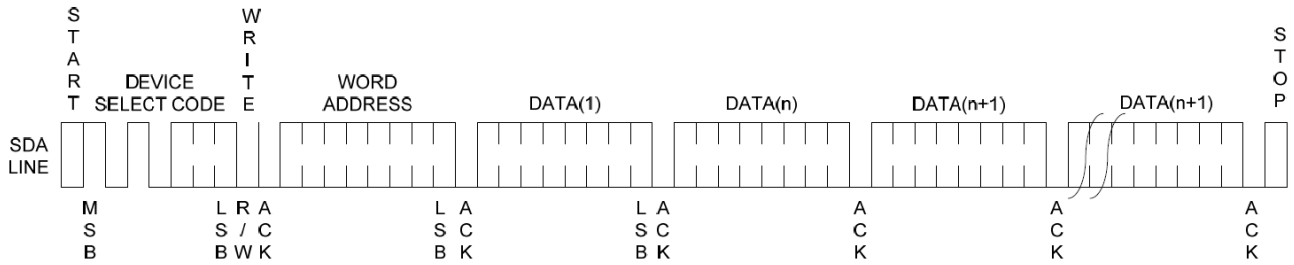


Figure 9. Page Write

Write Cycle Polling Using ACK

During the internal Write Cycle, the SPD EEPROM portion disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum write time (t_W) is shown in Table 24, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence of master, as shown in Figure 10, is:

Initial condition: a Write Cycle is in progress.

Step 1: The bus master issues a START condition followed by a Device Select Code of operate EEPROM (the first byte of the new instruction).

Step 2: If the device is busy with the internal Write Cycle, NACK will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write Cycle, it responds with an ACK, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

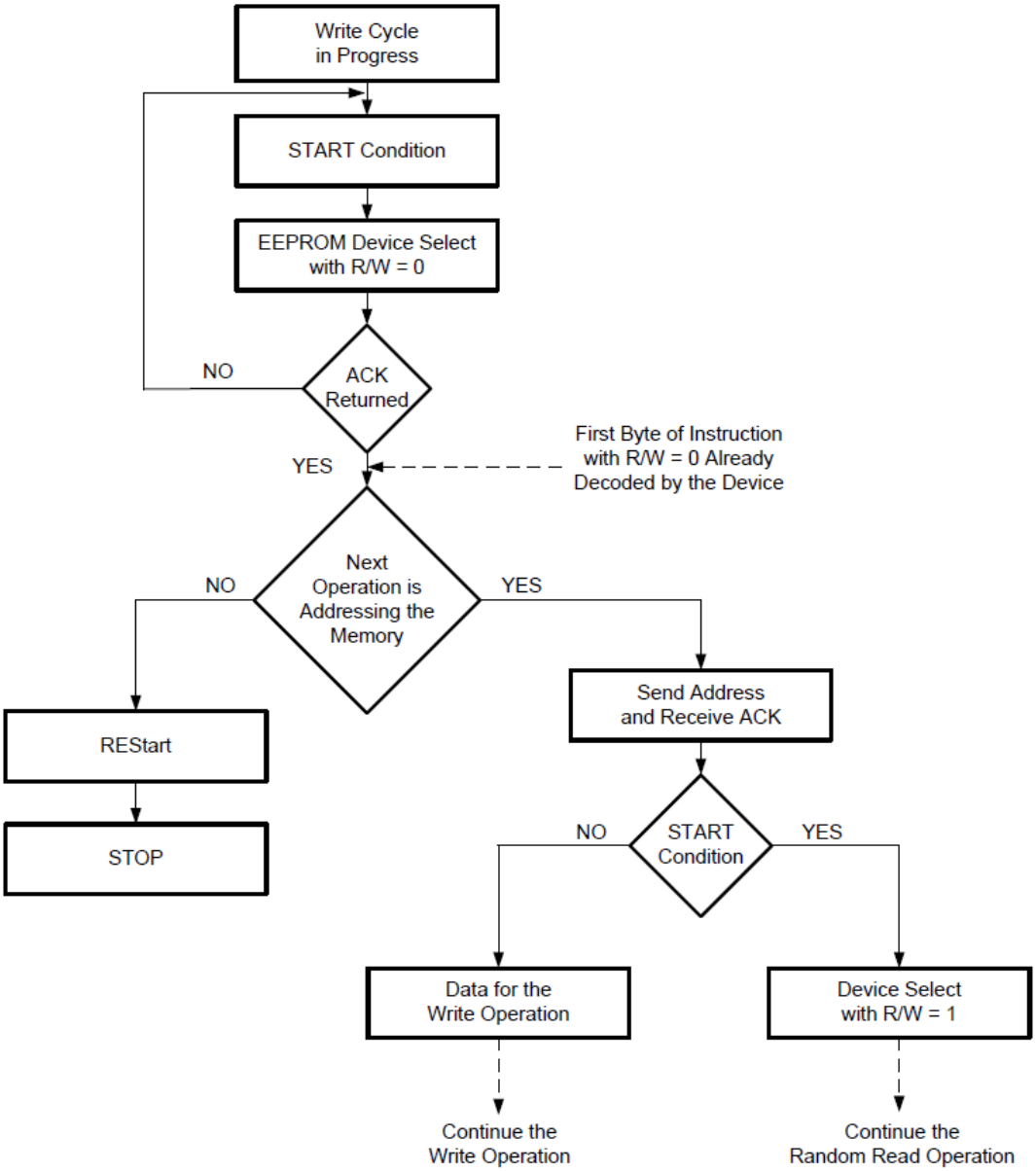


Figure 10. Write Cycle Polling Flowchart for EEPROM Using ACK

Read Operations

Read operations are performed independent of the software protection state, the device has an internal address counter which is incremented each time a byte is read.

Random Read

A dummy Write is first performed to load the Address into this address counter (as shown in Figure 11) but without sending a STOP condition. Then, the bus master sends another START (RESTART) condition, and repeats the Device Select Code, with the R/W bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must not acknowledge the byte, and terminates the transfer with a STOP condition.

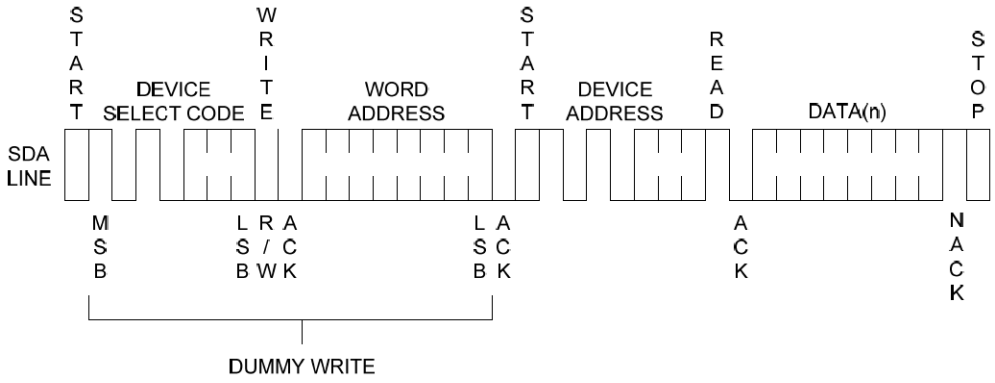


Figure 11. Random Read

Current Read

For the Current address Read operation, following a START condition, the bus master only sends a Device Select Code with the R/W bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a STOP condition, without acknowledging the byte, as shown in Figure 12.

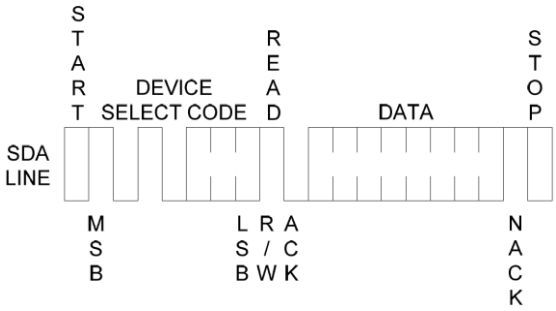


Figure 12. Current Read

Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master acknowledge the Data byte output, and sends additional clock pulses so that the device continues to output the next Data byte in sequence. To terminate the stream of Data bytes, the bus master must not acknowledge the last byte, and must generate a STOP condition, as shown in Figure 13.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 0x00.

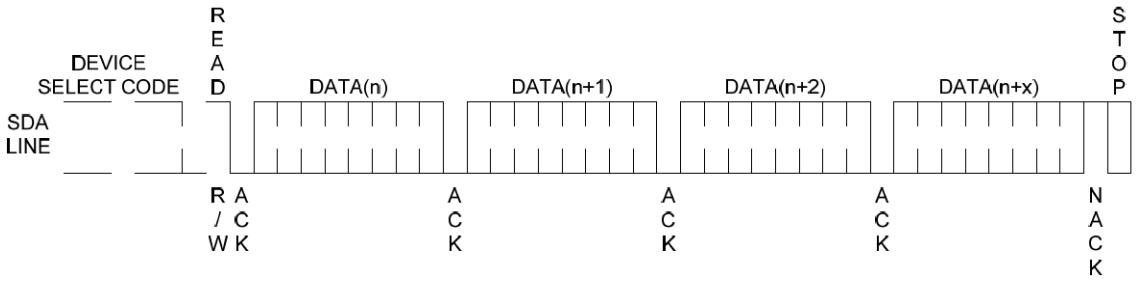


Figure 13. Sequential Read

Write Protection

There are four independent memory blocks, and each block may be independently protected. The memory blocks are:

Block 0: Memory addresses 0x00 to 0x7F, Page address = 0

Block 1: Memory addresses 0x80 to 0xFF, Page address = 0

Block 2: Memory addresses 0x00 to 0x7F, Page address = 1

Block 3: Memory addresses 0x80 to 0xFF, Page address = 1

The level of Write Protection (set or clear), that has been defined using these instructions, remains defined even after a Power Cycle.

SWPn: Set Write Protection for block n

CWP: Clear Write Protection for all blocks

RPSn: Read Protection status for block n

The SWP, CWP and RPS instructions are defined in Table 2.

All of the command such as SWPn, CWP, RPSn, SPAn, and RPA are the same command format, the Device Select Code is followed by a START condition from the master, the device replies to the master with ACK or NACK base on the actual state of itself, then the master sends one Address byte and one Data byte but the value of them are Not Significant (Don't Care), the device also need to replies to the master with ACK or NACK base on the actual status of itself separately.

The Protocol format sees Figure 14.

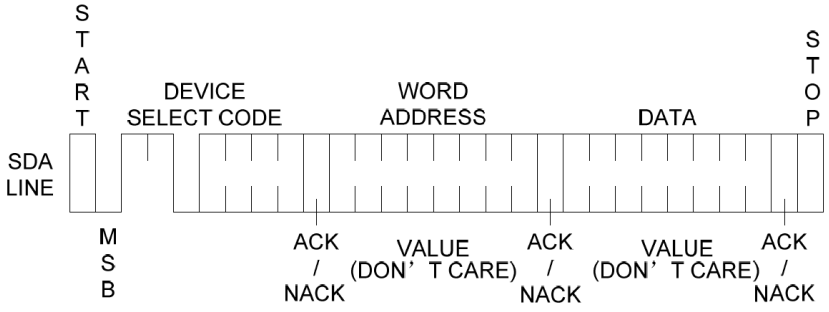


Figure 14. Protocol for Commands SWPn, CWP, RPSn, SPAn, RPA

Set and Clear the Write Protection (SWPn and CWP)

If the software Write Protection has been set with the SWPn instruction, it may be cleared again with a CWP instruction. SWPn acts on a single block as specified in the SWPn command, but CWP clears the Write Protection for all blocks.

When change the Write Protection, the Pin A0 of device must connect a high voltage V_{HV}, the level range of V_{HV} please see Table 23.

When decoded, SWPn and CWP trigger a Write Cycle lasting t_W (see Table 4).

Read Protection Status (RPSn)

The controller issues an RPSn command specifying which block to report upon. If the software Write Protection has not been set, the device replies to the Data byte with an ACK, and if it has been set, the device replies to the Data byte with a NACK.

When Read the Protection Status, the Pin A0 of device can connect 0, 1 or V_{HV}, and the Protection Status is no change on this operation.

Set SPD Page Address (SPAn)

The controller issues a SPAn command to select the lower 256 bytes (SPA0) or upper 256 bytes (SPA1). After a cold or warm POR, the SPD Page Address is always 0, selecting the lower 256 bytes.

Read SPD Page Address (RPA)

The controller issues an RPA command to determine if the currently selected SPD page is 0 (device returns ACK) or 1 (device returns NACK).

Acknowledge Expression

For all Read commands to the SPD, the device waits after each byte read, for an acknowledgment during the 9^{th} bit time. If the bus master does not drive SDA Low during this time, the device terminates the data transfer and returns to an idle state to await the next valid START condition, as shown in Table 4 and Table 5.

Table 4. Acknowledge when Writing Data or Defining Write Protection

Status	Instruction	Ack	Address	Ack	Data Byte	Ack	Write Cycle (tW)
Protected	SWPn	NACK	Not Significant	NACK	Not Significant	NACK	No
	CWP	ACK	Not Significant	ACK	Not Significant	ACK	Yes
	Page or Byte Write in Protected Block	ACK	Address	ACK	Data	NACK	No
Not Protected	SWPn or CWP	ACK	Not Significant	ACK	Not Significant	ACK	Yes
	Page or Byte Write	ACK	Address	ACK	Data	ACK	Yes

Table 5. Acknowledge when Reading the Protection Status

SWPn Status	Instruction	Ack	Address	Ack	Data Byte	Ack
Set	RPSn	NACK	Not Significant	NACK	Not Significant	NACK
Not Set	RPSn	ACK	Not Significant	NACK	Not Significant	NACK

Temperature Sensor Operation

The TS continuously monitors ambient temperature and updates to the temperature data register. Temperature data is latched internally by the device and may be read by software from the master at any time.

After initial POR, the configuration registers are set to the default values. The software can write to the configuration register to set limits register, configuration register and resolution register. All registers in the address space from 0x00 through 0x08 are 16-bit registers, accessed through I^2C Read and Write commands. Behavior on accesses to invalid register locations returns a NACK.

TS Write Operations

The registers in this device are selected by the pointer register. When power-up, the pointer register is set to '0x00'. The pointer register latches the last location it was set to. Each operation falls into one of two types of user accessibility:

1. Write to this device will always include the Device Select Code byte and the Pointer byte. The pointer register latches the data for reading operation (see Figure 15).
2. Write to TS register will always include the Device Select Code byte, the Pointer byte, and requires two Data bytes. The pointer register latches the data for reading operation (see Figure 16).

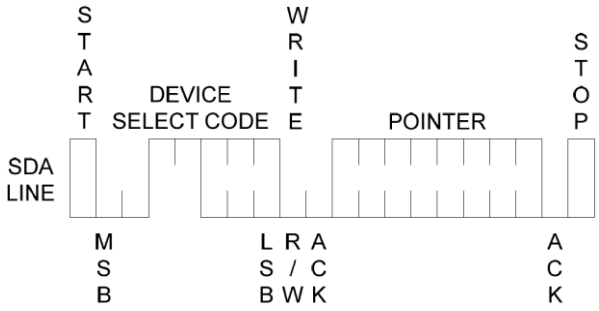


Figure 15. Write to Pointer Register

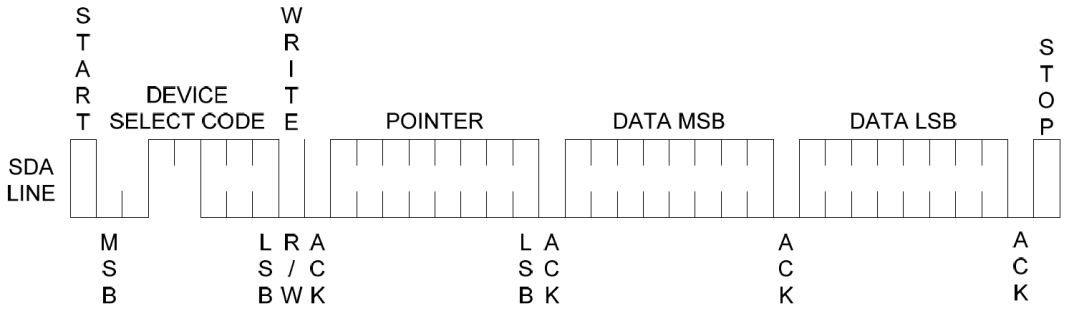


Figure 16. Write to TS Register

TS Read Operations

Reading ACE34LA04A is achieved in one of two ways:

1. If the location latched in the pointer register is correct (most of the time, it is expected that the pointer register will point to one of the read temperature registers because that will be the data most frequently read), then the Read can simply consist of an Device Select Code byte, followed by retrieval of the two Data bytes. See the Figure 17.

2. If the pointer register need to be set, then a Device Select Code byte, Pointer byte, RESTART, and another Device Select Code byte with R/W bit is set will accomplish a Read command. See the Figure 18. The Data byte transfers the MSB first. At the end of a Read, the master can send NACK and STOP to terminal the reading operation.

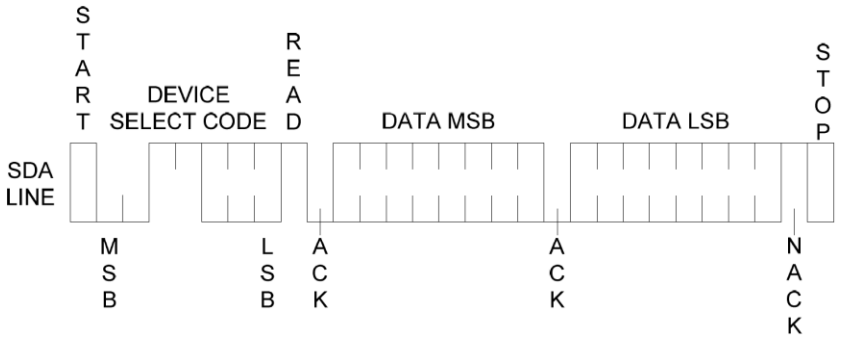


Figure 17. Preset Pointer Register Word Read

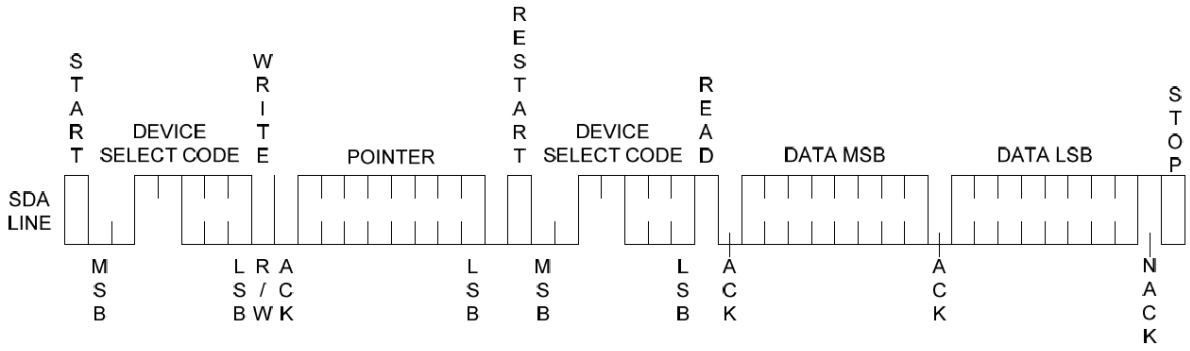


Figure 18. Pointer Write Register Word Read

Temperature Sensor Registers

The registers description is shown in Table 6.

Table 6. Temperature Register Addresses

Pointer Address	R/W	Name	Default
00	R	Capabilities Register	0x00EF
01	R/W	Configuration Register	0x0000
02	R/W	High Limit Register	0x0000
03	R/W	Low Limit Register	0x0000
04	R/W	TCRIT Limit Register	0x0000
05	R	Ambient Temperature Register	Undefined
06	R	Manufacturer ID Register	0x1860
07	R	Device/Revision Register	0x2201
08	R/W	Temperature Resolution Register	0x0001

Capabilities Register

The TS Capabilities Register indicates the supported features of the TS portion of the ACE34LA04A. This register is read-only and writing to it will have no effect. See Table 7.

Table 7. Capability Register Format

Pointer Address	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default Value
00	R	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU	0x00EF
		EVSD	TMOUT	VHV	TRES[1:0]		RANGE	ACC	EVENT	

Bits 15-8: RFU

Reserved for future, these bits will always read as '0'.

Bit 7: EVSD

‘0’: Not used.

‘1’: The EVENT_n output is de-asserted (not driven) when entering shutdown, and remains deasserted upon exit from shutdown until the next thermal sample is taken. In interrupt mode, EVENT_n may or may not be asserted when exiting shutdown if a pending interrupt has not been cleared.

Bit 6: TMOUT

Bus timeout function supported.

‘0’: Not used.

‘1’: Parameter $t_{TIMEOUT}$ is supported within the range of 25 to 35 mS.

Bit 5: VHV

‘0’: Not used.

‘1’: Support.

Bits 4-3: TRES [1:0]

Indicate the resolution of the temperature monitor. The ACE34LA04A resolution is programmable via writing to pointer 08 register, TRES of this register only indicate the status, the power on default value is 0.25°C/LSB (10-bit).

‘00’: 0.5 °C (9-bit).

‘01’: 0.25 °C (10-bit).

‘10’: 0.125 °C (11-bit).

‘11’: 0.0625 °C (12-bit).

Bit 2: RANGE

Indicate the supported temperature range.

‘0’: Values lower than 0°C will be clamped and represented as binary value '0'.

‘1’: Temperatures below 0°C can be read and the Sign bit will be set accordingly.

Bit 1: ACC

Indicate the supported temperature accuracy.

‘0’: Not used.

‘1’: The temperature monitor has ±1 °C accuracy over the active range (75°C to 95°C) and ±2°C accuracy over the monitoring range (40°C to 125°C).

Bit 0: EVENT

Indicate whether the temperature monitor supports interrupt capabilities.

‘0’: Alarm and critical trips turned OFF.

‘1’: Alarm and critical trips turned ON.

Configuration Register

The TS Configuration Register holds the control and status bits of the EVENT_n pin as well as general hysteresis on all limits. To avoid glitches on the EVENT_n output pin, users should disable EVENT or TCRIT functions prior to programming or changing other device configuration settings. See Table 8 for details.

Table 8. Configuration Register Format

Pointer Address	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default Value
01	RW	RFU	RFU	RFU	RFU	RFU	HYST[1:0]		SHDN	0x0000
		TCRIT_LOCK	EVENT_LOCK	CLEAR	EVENT_STS	EVENT_CTRL	TCRIT_ONLY	EVENT_POL	EVENT_MODE	

Bits 15-11: RFU

Reserved for future, these bits will always read '0' and writing to them will have no effect. For future compatibility, all RFU bits must be programmed as '0'.

Bits 10-9: HYST [1:0]

Control the hysteresis that is applied to all limits as shown in Table 9. This hysteresis applies to all limits register value when the temperature is dropping cross the given threshold, it must drop below the threshold minus the hysteresis in order to be flagged as an interrupt event. Note that hysteresis is also applied to EVENT_n pin functionality. When either of the lock bits is set, these bits cannot be altered.

Table 9. HYST Bit Decode

HYST[1:0]		HYSTERESIS
1	0	
0	0	Disable Hysteresis (default)
0	1	1.5°C
1	0	3°C
1	1	6°C

Bit 8: SHDN

Shut down. The thermal sensing device and ADC are disabled to save power, no events will be generated. When either of the lock bits (bit 7 and bit 6) is set, this bit cannot be set until unlocked. However it can be cleared at any time whether the lock bits are set or not. When in shutdown mode, ACE34LA04A devices still respond to commands normally. Default value is 0.

‘0’: The thermal sensor is active and converting.

‘1’: The thermal sensor is disabled and will not generate interrupts or update the temperature data.

Bit 7: TCRIT_LOCK

Lock the TCRIT Limit Register from being updated. Default value is 0.

‘0’: The TCRIT Limit Register can be updated normally.

‘1’: The TCRIT Limit Register is locked and cannot be updated. Once this bit has been set, it cannot be cleared until an internal POR.

Bit 6: EVENT_LOCK

Lock the High Limit and Low Limit Registers from being updated. Default value is 0.

‘0’: The High Limit and Low Limit Registers can be updated normally.

‘1’: The High and Low Limit Registers are locked and cannot be updated. Once this bit has been set, it cannot be cleared until an internal POR.

Bit 5: CLEAR

Clear the EVENT_n pin when it has been asserted. This bit is write-only and will always read '0'.

‘0’: Do nothing.

‘1’: The EVENT_n pin is released and will not be asserted until a new interrupt condition occurs. This bit is ignored if the device is operating in Comparator Mode. This bit is self clearing.

Bit 4: EVENT_STS

Indicate if the EVENT_n pin is asserted. This bit is read-only. Default value is 0.

‘0’: The EVENT_n pin is not being asserted by the device.

‘1’: The EVENT_n pin is being asserted by the device.

Bit 3: EVENT_CTRL

Mask the EVENT_n pin from generating an interrupt. If either of the lock bits (bit 7 and bit 6) is set, then this bit cannot be altered. Default value is 0.

‘0’: The EVENT_n pin is disabled and will not generate interrupts.

‘1’: The EVENT_n pin is enabled.

Bit 2: TCRIT_ONLY

Control whether the EVENT_n pin will be asserted from a High or Low out-of-limit condition. When the EVENT_LOCK bit (bit 6) is set, this bit cannot be altered. Default value is 0.

‘0’: The EVENT_n pin will be asserted if the measured temperature is above the High Limit or below the Low Limit in addition to if the temperature is above the TCRIT Limit.

‘1’: The EVENT_n pin will only be asserted if the measured temperature is above the TCRIT Limit.

Bit 1: EVENT_POL

Control the "active" polarity of the EVENT_n pin. The EVENT_n pin is driven to this polarity when it is asserted. If either of the lock bits (bit 7 and bit 6) is set, then this bit cannot be altered. Default value is 0.

‘0’: The EVENT_n pin is active low. The "active" state of the pin will be logical '0'.

‘1’: The EVENT_n pin is active high. The "active" state of the pin will be logical '1'.

Bit 0: EVENT_MODE

Control the behavior of the EVENT_n pin. The EVENT_n pin may function in either comparator or interrupt mode. If either of the lock bits (bit 7 and bit 6) is set, then this bit cannot be altered. Default value is 0.

‘0’: The EVENT_n pin will function in comparator mode.

‘1’: The EVENT_n pin will function in interrupt mode.

Temperature Register Value Format Definition

Temperatures in the High Limit Register, Low Limit Register, TCRIT Limit Register, and Temperature Data Register are expressed in 16-bit. Bit B12 through B2 for each of these registers are defined for all device resolutions as defined in the TRES field of the Capabilities Register and hence a 0.25°C minimum granularity is supported in all registers. Examples of valid settings and interpretation of temperature register bits are shown in Table 10.

Table 10. Temperature Register Coding Examples

B15~B0 (binary)(1)	Value	Units
xxx0_0000_0010_11xx	2.75	°C
xxx0_0000_0001_00xx	1	°C
xxx0_0000_0000_01xx	0.25	°C
xxx0_0000_0000_00xx	0	°C
xxx1_1111_1111_11xx	–0.25	°C
xxx1_1111_1111_00xx	–1.00	°C
xxx1 1111 1101 11xx	–2.25	°C
xxx1 1110 1100 00xx	–20.00	°C

Note: (1). For 10 bit resolution

The TRES field of the Capabilities Register optionally defines higher resolution devices. For compatibility and simplicity, this additional resolution affects only the Temperature Data Register but none of the Limit Registers. When higher resolution devices generate status or EVENT_n changes, only bits B12 through B2 are used in the comparison; however, all 11 bits (TRES[1:0] = 2'b10) or all 12 bits (TRES[1:0] = 2'b11) are visible in reads from the Temperature Data Register.

When a lower resolution device is indicated in the Capabilities Register (TRES [1:0] = 2'b00), the finest resolution supported is 0.5°C. When this is detected, bit 2 of all Limit Registers should be programmed to 0 to assure correct operation of the temperature comparators.

Limit Register

The Temperature Limit Registers (High Limit, Low Limit, and TCRIT Limit) define the temperatures to be used by various on-chip comparators to determine device temperature status and thermal EVENT. For future compatibility, unused bits '-' must be programmed as 0.

High Limit Register

The High Limit Register holds the High Limit for the nominal operating window. When the temperature rises above the High Limit, or drops below or equal to the High Limit minus the hysteresis, then the EVENT_n pin is asserted (if enabled). If the EVENT_LOCK bit is set in the Configuration Register, this register becomes read-only. See Table 11 for details.

Table 11. High Limit Register

Pointer Address	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default Value
02	RW				Sign	128	64	32	16	0x0000
		8	4	2	1	0.5	0.25			

Low Limit Register

The Low Limit Register holds the lower limit for the nominal operating window. When the temperature drops below the Low Limit minus the hysteresis or rises up to meet or exceed the Low Limit, then the EVENT_n pin is asserted (if enabled). If the EVENT_LOCK bit is set in the Configuration Register, this register becomes read-only. See Table 12 for details.

Table 12. Low Limit Register

Pointer Address	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default Value
03	RW	-	-	-	Sign	128	64	32	16	0x0000
		8	4	2	1	0.5	0.25	-	-	

TCRIT Limit Register

The TCRIT Limit Register holds the TCRIT Limit. If the temperature exceeds the limit, the EVENT_n pin will be asserted. It will remain asserted until the temperature drops below or equal to the limit minus the hysteresis. If the TCRIT_LOCK bit is set in the Configuration Register, this register becomes read- only. See Table 13 for details.

Table 13. TCRIT Limit Register

Pointer Address	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default Value
04	RW	-	-	-	Sign	128	64	32	16	0x0000
		8	4	2	1	0.5	0.25	-	-	

Temperature Data Register

The Temperature Data Register holds the data and sign for the internal temperature measurement as well as the status bits indicating which limit conditions. The encoding of bits B12 through B2 are the same as the temperature limit registers, B1 and B0 indicate the 0.125°C and 0.0625°C separately, and B2 through B0 defined base on value of TRES field of the Capabilities Register, Unused or unsupported bits will read as 0. This register has no default value, write data to this register can't change the temperature data. See Table 14 for details.

Table 14. Temperature Data Register

Pointer Address	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default Value
05	R	TCRIT	HIGH	LOW	Sign	128	64	32	16	Undefined
		8	4	2	1	0.5	0.25	0.125	0.0625	

Bit 15: TCRIT

Once set, the temperature is above the TCRIT Limit. This bit will remain set so long as the temperature is above TCRIT and will automatically clear once the temperature has dropped below or equal the limit minus the hysteresis.

Bit 14: HIGH

Once set, the temperature is above the High Limit. This bit will remain set so long as the temperature is above the HIGH limit and it will only be cleared when the temperature drops below or equal to the HIGH Limit minus the hysteresis.

Bit 13: LOW

Once set, the temperature is below the Low Limit minus the hysteresis. This bit will remain set so long as the temperature is below the Low Limit minus the hysteresis and it will only be cleared when the temperature meets or exceeds the Low Limit.

Manufacturer ID Register

The Manufacturer's ID (programmed value 1860h) in this register is the ACE's Identification provided by the Peripheral Component Interconnect Special Interest Group (PCI-SIG), See Table 15.

Table 15. Manufacturer ID Register

Pointer Address	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default Value
06	R	0	0	0	1	1	0	0	0	0x1860
		0	1	1	0	0	0	0	0	

Device ID and Device Revision ID Register

The Device ID and Device Revision ID are maintained in this register. The register format is shown in Table 16. The Device ID and Device Revision ID reflect the current device. The current Device ID and Device Revision ID value is 2201h.

Table 16. Device ID and Device Revision ID Register

Pointer Address	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default Value
07	R	0	0	1	0	0	0	1	0	0x2201
		0	0	0	0	0	0	0	1	

Temperature Resolution Register

With this register, user can program the TS resolution from 9 to 12 bit as shown in Table 17 and Table 18. The power on default is always 10 bit (0.25°C/LSB). The selected resolution is also reflected in bits TRES of the Capability Register.

Table 17. Temperature Resolution Register

Pointer Address	R/W	B15/B7	B14/B6	B13/B5	B12/B4	B11/B3	B10/B2	B9/B1	B8/B0	Default Value
08	R	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU	0x0001
		RFU	RFU	RFU	RFU	RFU	RFU	Resolution Bits		

Table 18. Resolution Bits Details

Resolution register Bits		Resolution Bit	°C/LSB	Conversion Time (max)
Bit1	Bit0			
0	0	9	0.5	65 mS
0	1	10	0.25	125 mS (default)
1	0	11	0.125	250 mS
1	1	12	0.0625	500 mS

Use Within DDR4 DIMM Module

The I^2C slave address selection pins allow up to 8 such devices to co-exist on the same bus. This means that up to 8 memory modules can be supported, given that each module has one such slave device address slot.

In the application, the ACE34LA04A is soldered directly in the DIMM PCB module. The three slave address inputs (A2, A1, A0) must be connected to GND or V_{CC} directly (that is without using a serial resistor) through the DRAM module connector (see Table 19 and Figure 19). The pull up resistor on SDA is connected on the SMBus of the motherboard.

Table 19. DIMM Module Slave Address Configuration

DIMM Position	A2	A1	A0
0	GND	GND	GND
1	GND	GND	V_{CC}
2	GND	V_{CC}	GND
3	GND	V_{CC}	V_{CC}
4	V_{CC}	GND	GND
5	V_{CC}	GND	V_{CC}
6	V_{CC}	V_{CC}	GND
7	V_{CC}	V_{CC}	V_{CC}

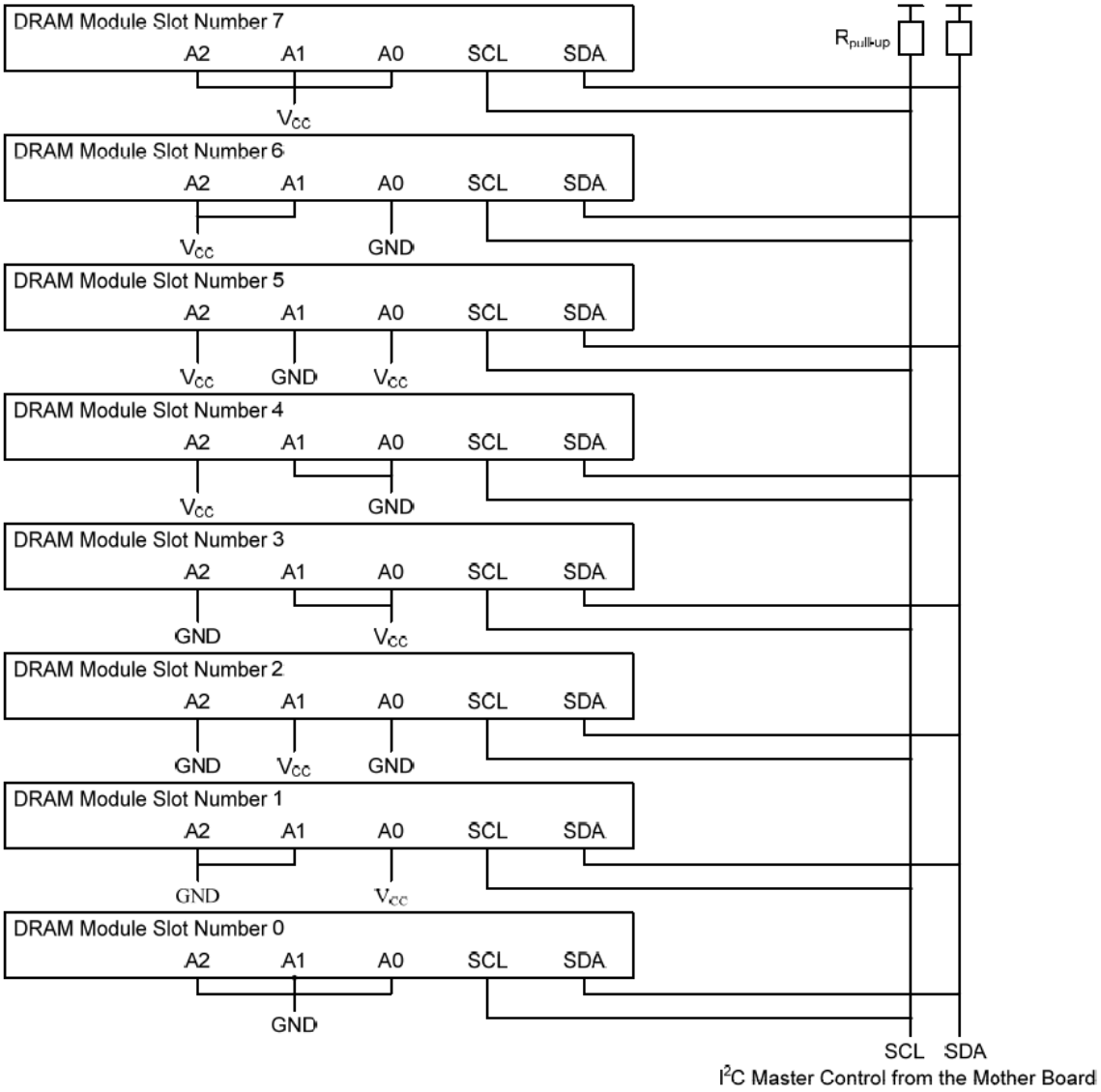


Figure 19. Address Configuration on the Mother Board

Programming

The ACE34LA04A is programmed can be considered in three situations.

SPD Device is Isolated

When the SPD device is isolated, not soldered on the DIMM PCB, generally, it is used in factory mode or programming before used the device. With specific programming equipment, it is possible to define the ACE34LA04A content, using Byte Write or Page Write instructions, and the Write Protection SWPn and CWP instructions. To issue the SWPn and CWP instructions, the signal applied on SA0 must be driven to V_{HV} during the whole instruction.

DIMM is Isolated

When the DDR4 DIMM is isolated, SPD device is soldered on the DIMM PCB and DIMM not inserted on the motherboard. It is programmed in the same method with SPD device is isolated but the specific programming equipment must with DIMM interface connector.

DIMM is Loaded

When the DDR4 DRAM is inserted on the motherboard, generally, it is used in application programming. Table 4 and Table 5 show how the ACK bits can be used to identify the Write Protection status.

Characteristics

Maximum Ratings

Stresses follow those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability. See Table 20 for details.

Table 20. Absolute Maximum Rating

Symbol	Parameter		Value	Unit
T_{STG}	Storage Temperature		-65 to 150	°C
T_{SLD}(1)	Lead Solder Temperature for 10 Seconds		260	°C
V_{IO}	Input or Output Voltage	A0	-0.3 ~ 10.0	V
		Others	-0.3 ~ 4.3	V
V_{CC}	Supply Voltage		-0.3 ~ 4.3	V
I_O	Output Current		10	mA
θ_{JA}	Thermal Resistance		89	°C/W

DC and AC Parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the devices. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters. See Table 21, Figure 20, Table 22 and Table 23 for details.

Table 21. Operating and AC Measurement Condition

Parameter		Conditions	Unit
V_{CC} Supply Voltage	TS	2.2 ~ 3.6	V
	EE	1.7 ~ 3.6	V
Operating Temperature		–40 to 125	°C
Input Rise and Fall Times		≤50	nS
Load Capacitance		100	pF
Input Pulse Voltages		$0.2V_{CC}$ to $0.8V_{CC}$	V
Input and Output Timing Reference Voltages		$0.3V_{CC}$ to $0.7V_{CC}$	V

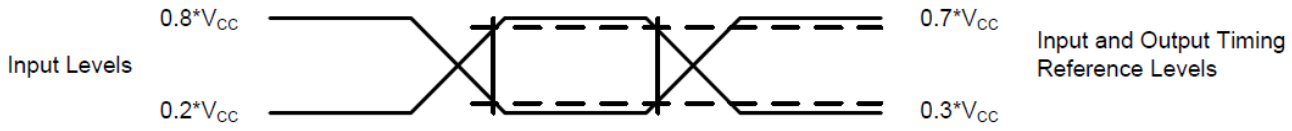


Figure 20. AC Measurement I/O Waveform

Table 22. Input Parameter

Symbol	Description(1)	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance(A0,A1,A2,SCL)	V_{IN} = 0V		6	pF
$C_{I/O}$	Input and Output Capacitance(SDA)	V_{IO} = 0V		8	pF
Z_{AIL}	A0, A1, A2 Input Impedance	V_{IN} < 0.3 V_{CC}	30		KΩ
Z_{AIH}	A0, A1, A2 Input Impedance	V_{IN} > 0.7V_{CC}	800		KΩ
t_{SP}	Spike Suppression Pulse Width of Spikes that must be Suppressed by the Input Filter on SCL and SDA			50	nS

Note: (1). Verified by design and characterization, not necessarily tested on all devices.

Table 23. DC Characteristics

Symbol	Description	Test Condition(1)	Min	Typ(2)	Max	Unit
V_{CC}	Supply Voltage	TS	2.2	3.3	3.6	V
		EE	1.7	3.3	3.6	V
I_{DD}	V_{CC} Supply Current (no load)	EEPROM Active(3) f = 1000 KHz		0.4	0.8	mA
		EEPROM Standby, f = 1000 KHz		160	450	µA
I_{DDW}	V_{CC} Supply Current (Write)	V_{CC} = 3.3 V, f = 1000 kHz(4)			0.7	mA
I_{DD1}	Shutdown Mode Supply Current	EEPROM Standby, TS Shutdown		0.1	0.5	µA
I_{ILI}	Input Leakage Current (SCL, SDA)	V_{IN} = GND or V_{CC}			±5	µA
I_{ILO}	Output Leakage Current	V_{OUT} = GND or V_{CC}, SDA in Hi-Z			±5	µA
V_{IL}	Input Logic Low	SCL, SDA, A0-A2	-0.5		$0.3V_{CC}$	V
V_{IH}	Input Logic High	SCL, SDA, A0-A2	$0.7V_{CC}$		V_{CC}+1.0	V
V_{HV}	A0 High Voltage	V_{HV} ≥V_{CC} +4.8 V	7		10	V
V_{OL1}	Output Low Voltage	I_{OL} = 3.0 mA, V_{CC} > 2.2 V			0.4	V
I_{OL}	Low Level Output Current	V_{OL} = 0.4 V	20			mA
V_{HYST}	Input Hysteresis (SCL, SDA)	V_{CC} < 2.0 V	$0.1V_{CC}$			V
		V_{CC} ≥ 2.0 V	$0.05V_{CC}$			V
V_{PON}	Power on Reset (POR) Threshold	Monotonic Rise between V_{PON} and V_{CC} (min) without Ring Back	1.6			V
V_{POFF}	Power off Threshold for Warm Power on Cycle				0.9	V
V_{PU}	EVENT_n Pin Pull-up Voltage				V_{CC}+1.0	V

Note: (1).Guaranteed operating temperature for combined module: T_A=–40°C to 125°C; V_{CC}=2.2V to 3.6V (except where noted).

(2).Typical numbers taken at V_{CC}=3.3V, T_A=25°C.

(3).Read current only.

(4).Verified by design and characterization, not necessarily tested on all devices.

Timing Parameters

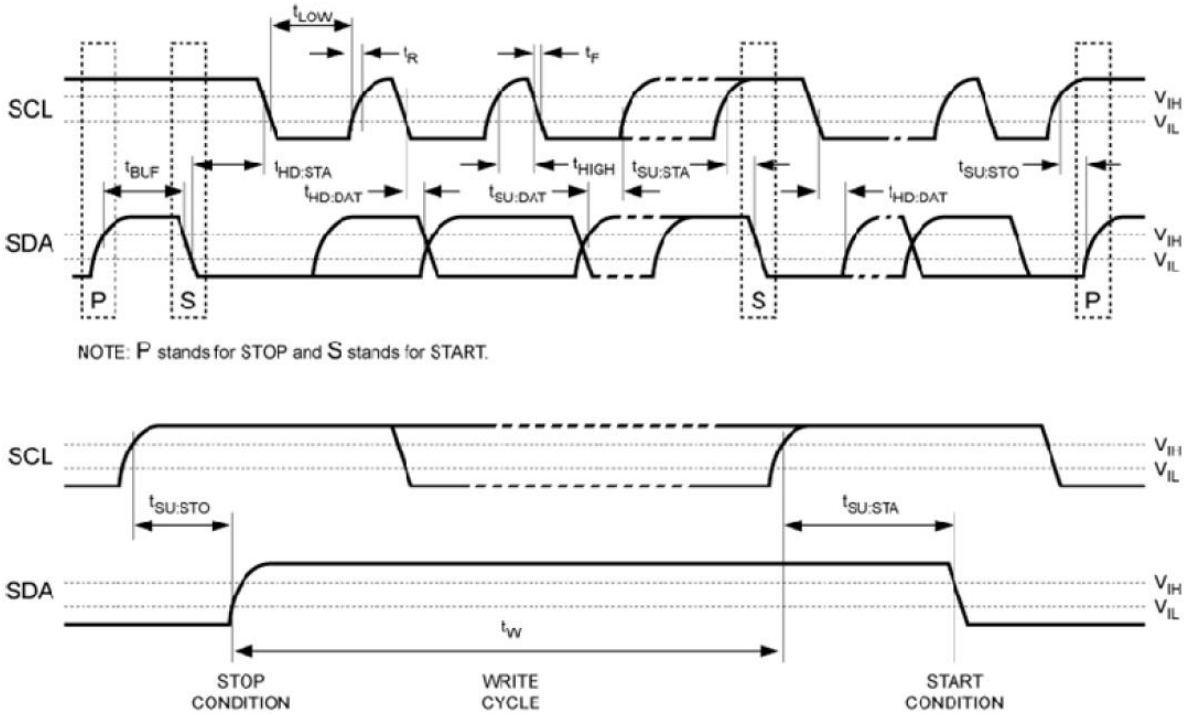


Figure 21. SMBus and I²C Timing Diagram

Table 24. SMBus and I²C Compatibility Timing

Symbol	Description(1)	Min	Max	Unit
f_{SCL}	I²C Clock Frequency	10	1000	KHz
t_{HIGH}	Clock High Period	260		nS
t_{LOW}(1)	Clock Low Period	500		nS
t_R	Clock and Data Rise Time		120	nS
t_F	Clock and Data Fall Time		120	nS
$t_{SU:DAT}$	Data-in Setup Time	50		nS
$t_{HD:DI}$	Data-in Hold Time	0		nS
$t_{HD:DAT}$	Data-out Hold Time	0	350	nS
$t_{SU:STA}$(2)	(RE) START Condition Setup Time	260		nS
$t_{HD:STA}$	Hold Time after (RE) START Condition. After this Period, the First Clock Cycle is Generated	260		nS
$t_{SU:STO}$	STOP Condition Setup Time	260		nS
t_{BUF}	Bus Free Time between STOP (P) and START (S) Conditions	500		nS

Symbol	Description(1)	Min	Max	Unit
t_W(3)	Write Time for EEPROM		3	mS
$t_{TIMEOUT}$(4)	Bus Timeout	25	35	mS
t_{POFF}	Warm Power Cycle off Time	1		mS
t_{INIT}	Time from Power-on to First Command	10		mS

Note:

(1). The ACE34LA04A will not initiate clock stretching which is an I^2C bus optional feature.

(2). For a RESTART condition, or following a Write Cycle.

(3). This parameter reflects maximum Write time for EEPROM.

(4). The I^2C bus masters can terminate a transaction in process and reset devices on the bus by asserting SCL low for $t_{TIMEOUT(MAX)}$ or longer. The ACE34LA04A, upon detecting this condition, will reset communication and be able to receive a new START condition no later than $t_{TIMEOUT\ (MAX)}$. The ACE34LA04A will not reset if SCL stretching is less than $t_{TIMEOUT\ (MIN)}$.

Temperature to Digital Performance

Table 25. Temperature to Digital Converter Performance

Symbol	Description	Test Condition	Min	Typ	Max	Unit
B-Grade	Accuracy for Corresponding Range 2.2V ≤ V_{CC} ≤ 3.6V	75°C < T_A < 95		±0.5	±1.0	°C
		40°C < T_A < 125		±1.0	±2.0	°C
		- 20°C < T_A < 125		±2.0	±3.0	°C
	Resolution		0.5	0.25	0.0625	°C/LSB
	Analog to Digital Converter		9	10	12	bit
t_{CONV}	Conversion Time	10-bit (default)		70	125	mS

R_{PU} Parameters

In DIMM applications, maximum external pull-up resistors on signals are specified see Figure 22, Line capacitance limitations should be calculated using the $R_{PU} \times C_{BUS}$ time constant must be below the 150 nS time constant line at maximum frequency f_C = 1 MHz.

Cap	Res
50 pF	2833 Ω
100 pF	1416 Ω
150 pF	944 Ω
200 pF	708 Ω
250 pF	567 Ω
300 pF	472 Ω
350 pF	405 Ω
400 pF	354 Ω
450 pF	315 Ω
500 pF	283 Ω
550 pF	258 Ω

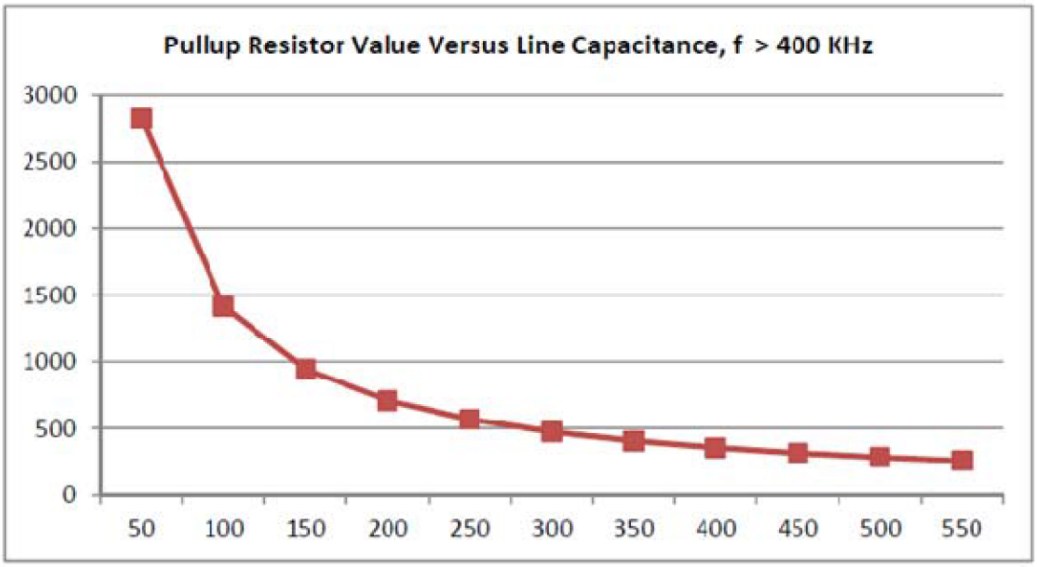
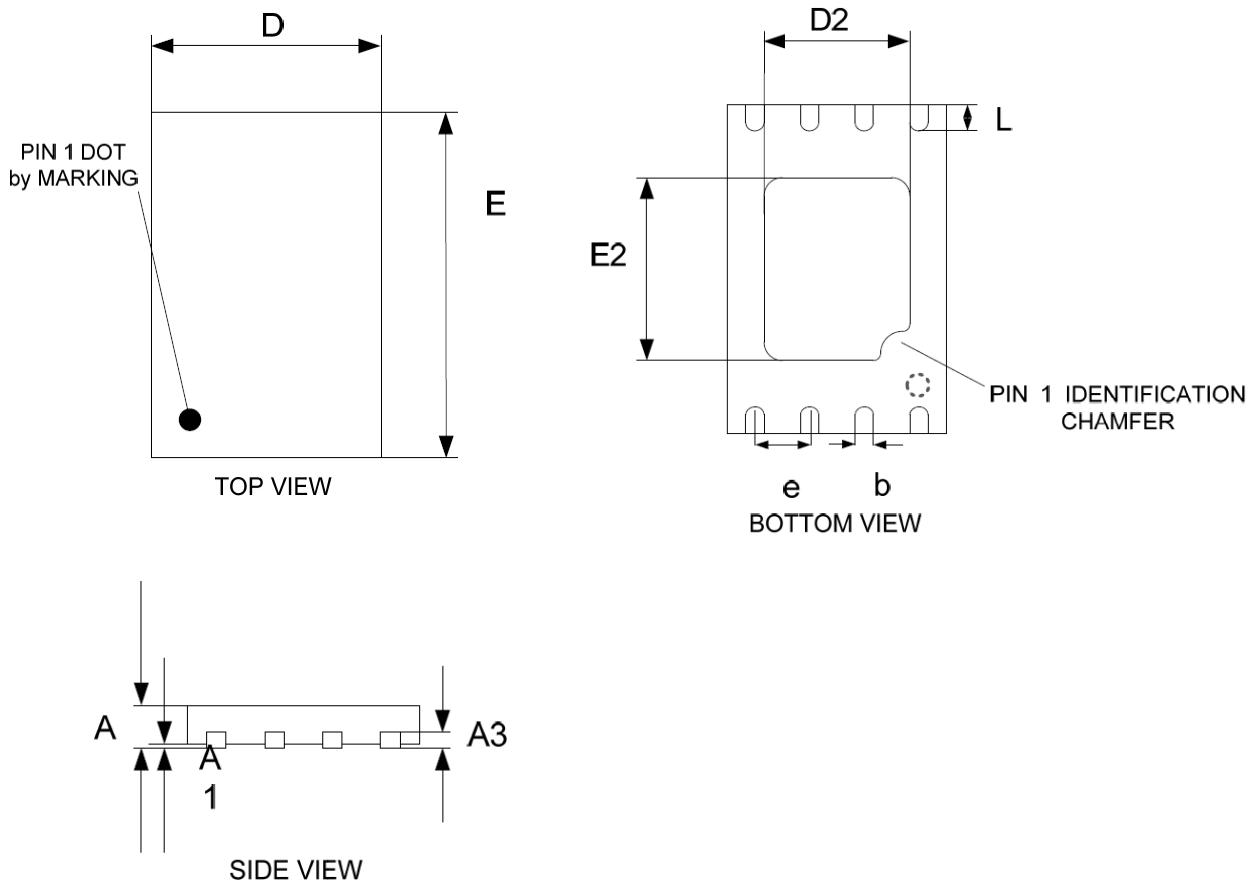


Figure 22. Pullup Resistor Value vs. Line Capacitance

Packaging Information

UDFN8



Common Dimension (MM)			
PKG	UT:Ultra Thin		
REF	MIN	NOM	MAX
A	>0.50	0.55	0.60
A1	0.00		0.05
A3	0.15 REF		
D	1.95	2.00	2.05
E	2.95	3.00	3.05
b	0.20	0.25	0.30
L	0.20	0.30	0.40
D2	1.25	1.40	1.50
E2	1.15	1.30	1.40
e	0.50 BSC		

Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Technology Co., LTD. As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and shoes failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.