ACE24LA512A
Two-wire Serial EEPROM

Description

The ACE24LA512A provides 524288 bits of serial electrically erasable and programmable read- only memory (EEPROM), organized as 65536 words of 8 bits each.

The device is optimized for use in many industrial and commercial applications where ow-power and low-voltage operation are essential.

The ACE24LA512A offers an additional page, named the Identification Page (128 bytes). The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

Features

- Compatible with all I2C bidirectional data transfer protocol
- Memory array:
  512 Kbits (64 Kbytes) of EEPROM
  Page size: 128 bytes
  Additional Write lockable page
- Single supply voltage and high speed:
  1 MHz
- Random and sequential Read modes
- Write:
  Byte Write within 3 ms
  Page Write within 3 ms
  Partial Page Writes Allowed
- Write Protect Pin for Hardware Data Protection
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- High-reliability
  Endurance: 1 Million Write Cycles
  Data Retention: 100 Years
- Enhanced ESD/Latch-up protection
  HBM 8000V
- 8-lead DIP/SOP/TSSOP and USON3*2-8 packages

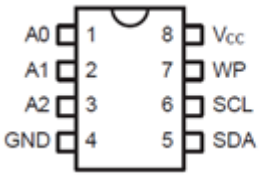
Absolute Maximum Ratings

DC Supply Voltage	-0.3V to 6.5V
Input / Output Voltage	GND-0.3V to V_{CC}+0.3V
Operating Temperature	-40℃ to 85℃
Storage Temperature	-65℃ to 150℃
Electrostatic pulse (Human Body model)	8000V

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Packaging Type

SOP-8



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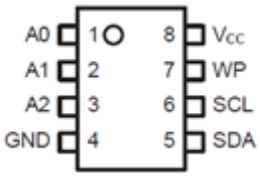

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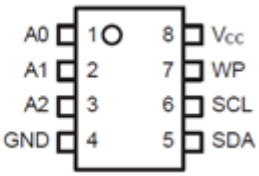
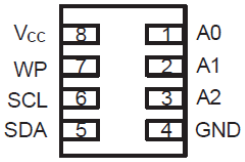


USON3*2-8



Pin Configurations

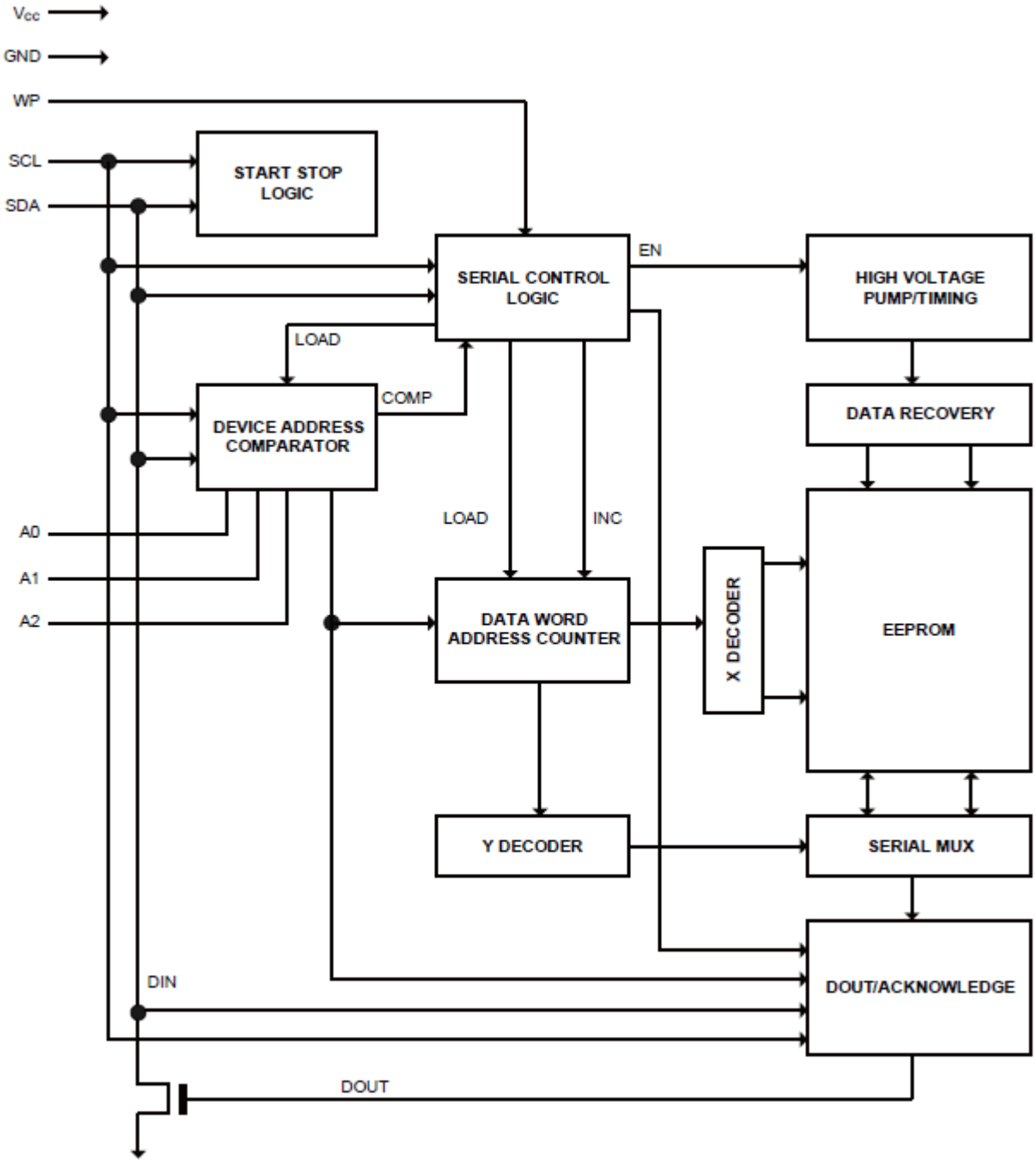
Pin Name	Type	Functions
AO-A2	I	Address Inputs
SDA	I/O	Serial Data
SCL	I	Serial Clock Input
WP	I	Write Protect
GND	P	Ground
V_{CC}	P	Power Supply

Ordering information

ACE24LA512A XX + X H

- Halogen-free
- U : Tube
  T : Tape and Reel
- Pb - free
- FM: SOP-8
  TM: TSSOP-8
  DP: DIP-8
  UA8: USON3*2-8

Block Diagram



Pin Descriptions

Device/Page Addresses (A2, A1 and A0):

The A2, A1 and A0 pins are device address inputs that are hard wire for the ACE24LA512A. Eight 512K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

Serial Data (SDA):

The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open- collector devices.

Serial Clock (SCL):

The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Write Protect (WP):

The ACE24LA512A has a Write Protect pin that provides hardware data protection.

The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protection pin is connected to Vcc, the write protection feature is enabled and operates as shown in the following Table 1.

Table 1. Write Protect

WP Pin Status	Part of the Array Protected
	ACE24LA512A
At V_{CC}	Full (512K) Array
At GND	Normal Read / Write Operations

Memory Organization

ACE24LA512A, 512K Serial EEPROM:

Internally organized with 512 pages of 128 bytes each, the 512K requires a 16-bit data word address for random word addressing.

Device Operation

Clock and Data Transitions:

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

Start Condition:

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 2).

Stop Condition:

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 2).

Acknowledge:

All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

Standby Mode:

The ACE24LA512A features a low-power standby mode which is enabled: (a) upon power- up and (b) after the receipt of the STOP bit and the completion of any internal operations.

Memory Reset:

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high and then.
3. Create a start condition.

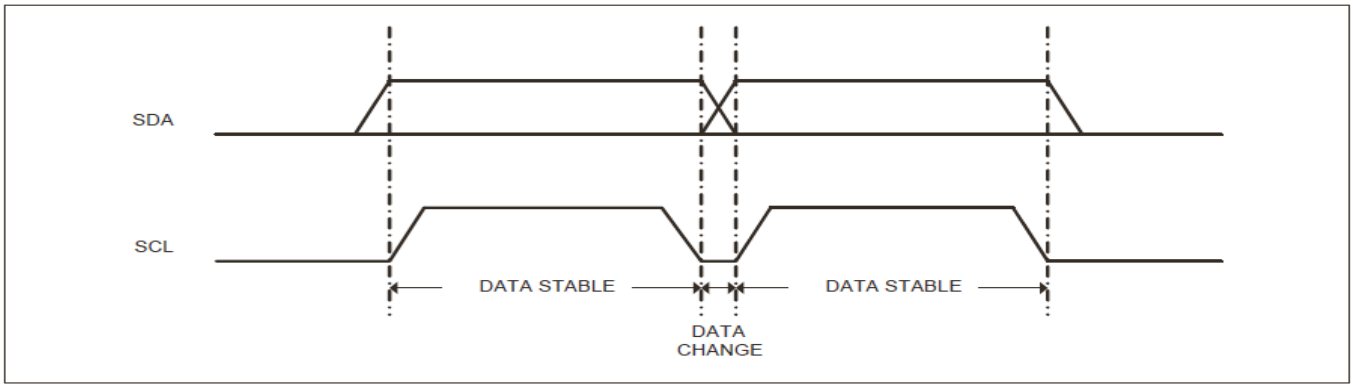


Figure 1: Data Validity

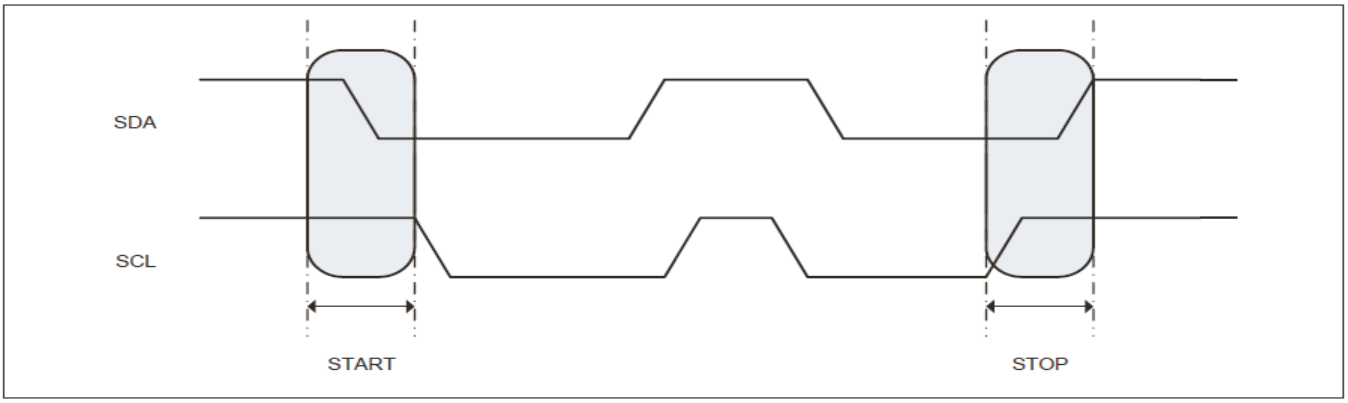


Figure 2: Start and Stop Definition

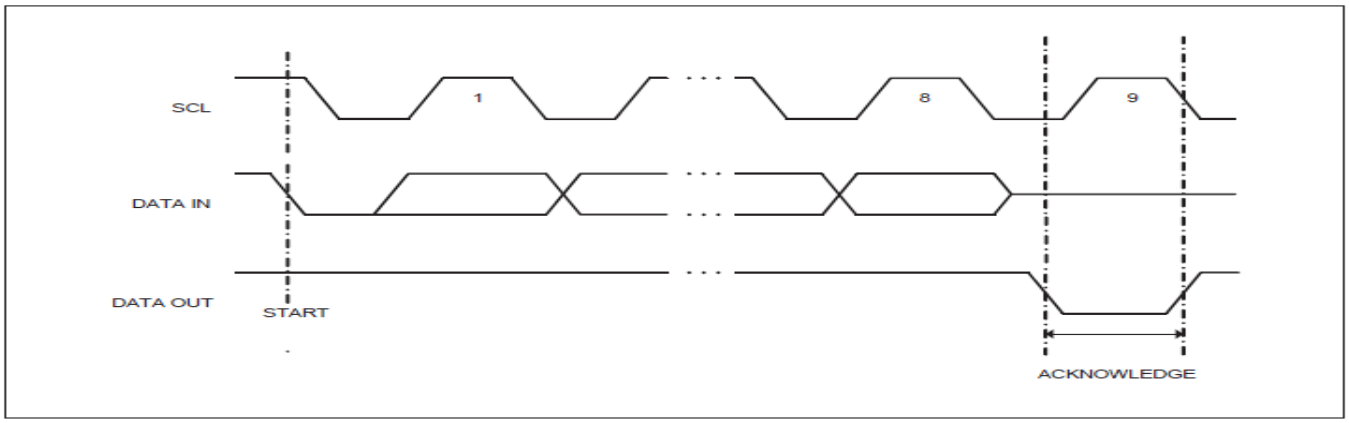


Figure 3: Output Acknowledge

Device Addressing

The 512K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 4)

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The 512K EEPROM uses A2, A1 and A0 device address bits to allow as much as eight devices on the same bus. These 3 bits must be compared to their corresponding hardwired input pins. The A2, A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

Data Security: The ACE24LA512A has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at VCC.

Write Operations

Byte Write:

A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, tWR, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 5).

Page Write:

A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, tWR, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 6).

The data word address lower five bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 128 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

Acknowledge Polling:

The Identification Page (128 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by issuing the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier = 1011b
- MSB address bits B15/B7 are don't care except for address bit B10 which must be "0". LSB address bits B5/B0 define the byte address inside the Identification page.

  If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoAck).

Acknowledge Polling:

Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

Current Address Read:

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 7).

Random Read:

A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 8)

Sequential Read:

Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see Figure9).

Read Identification Page: The Identification Page (128 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

The Identification Page can be read by issuing an Read Identification Page instruction. This instruction uses the same protocol and format as the Random Address Read (from memory array) with device type identifier defined as 1011b. The MSB address bits B15/B6 are don't care, the LSB address bits B5/B0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g.: when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 118, as the ID page boundary is 128 bytes)

Lock Identification Page: The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

Device type identifier = 1011b

Address bit B10 must be ‘1’; all other address bits are don't care

The data byte must be equal to the binary value xxxx xx1x, where x is don't care

Table 2.First Word Address

B15	B14	B13	B12	B11	B10	B9	B8

Table 3.Second Word Address

B7	B6	B5	B4	B3	B2	B1	B0

MSB							**LSB**
1	0	1	0	A2	A1	A0	R/W

Figure 4: Device Address

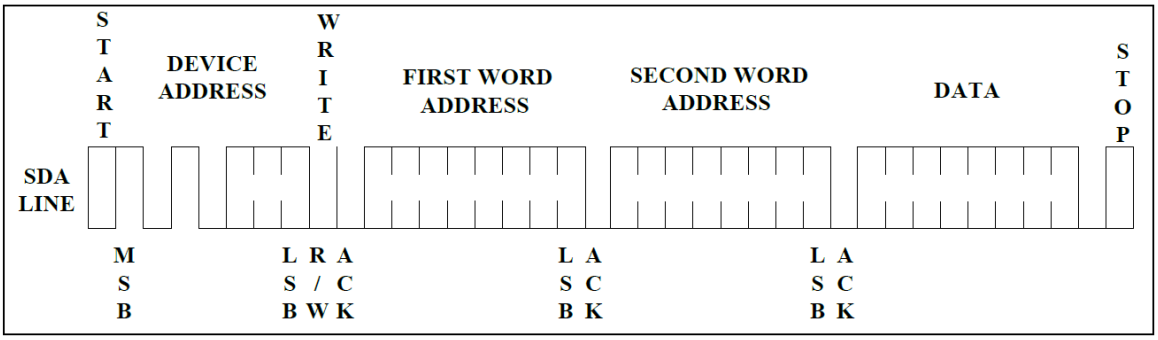


Figure 5: Byte write

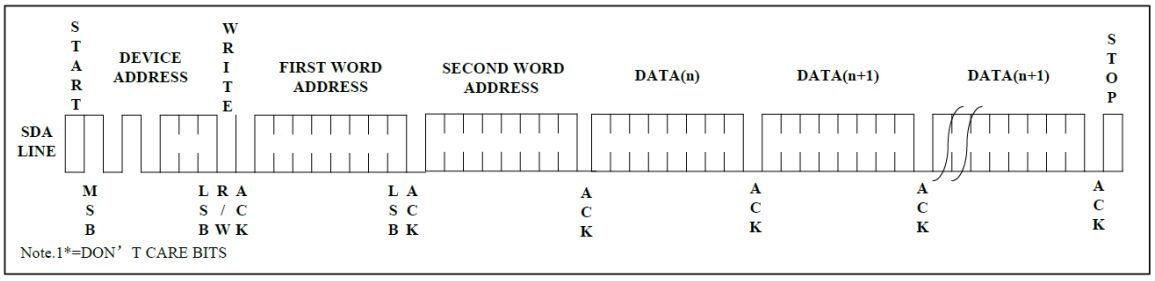


Figure 6: Page write

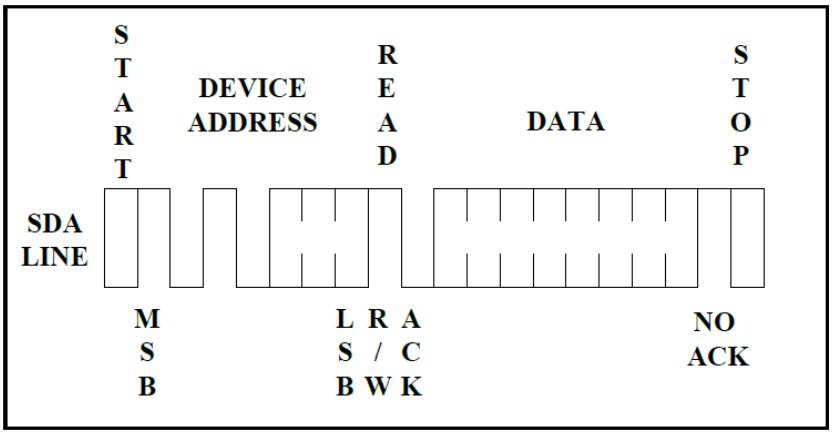


Figure 7: Current Address Read

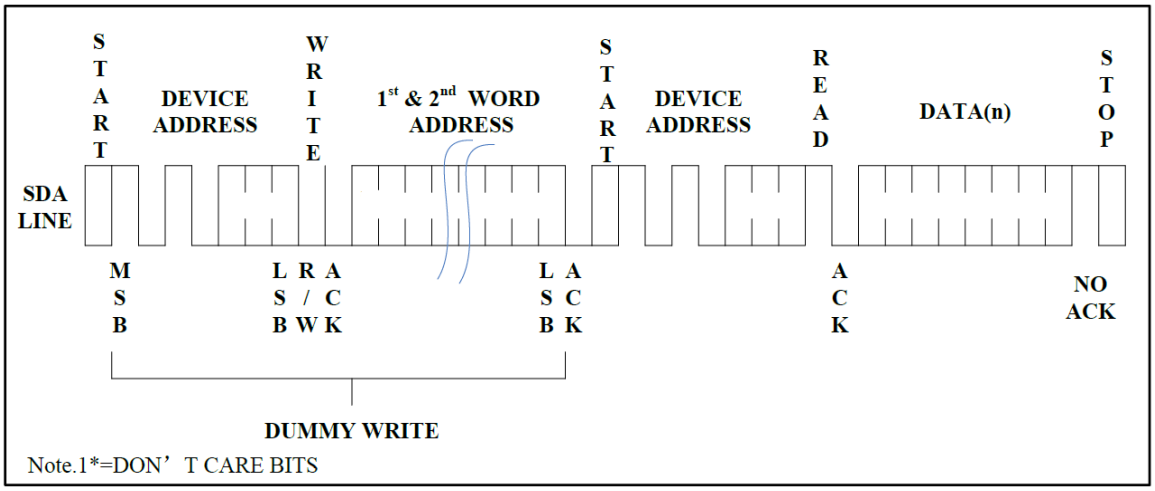


Figure 8: Random Read

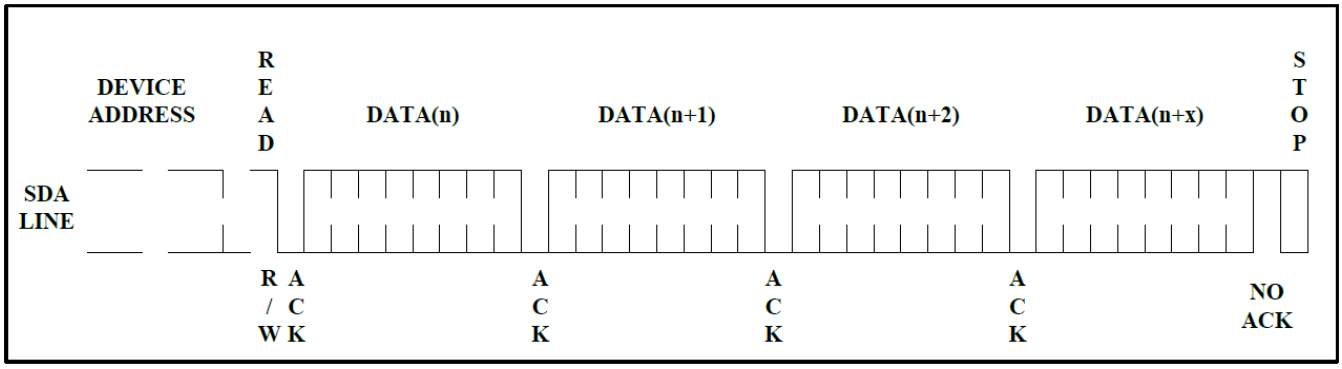


Figure 9: Sequential Read

Pin Capacitance

Applicable over recommended operating range from: T_A = 25℃, f = 1.0 MHz, V_{CC} = +1.7V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input / Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

DC Characteristics

Applicable over recommended operating range from: T_A = -40℃ to +85℃, V_{CC} = +1.7V to +5.5V, (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.7		5.5	V
V_{CC2}			2.5		5.5	
I_{CC1}	Supply Current V_{CC}=5.0V	Read at 400kHz		0.14	0.3	mA
I_{CC2}	Supply Current V_{CC}=5.0V	Write at 400 kHz		0.09	0.3	mA
I_{SB1}	Standby Current V_{CC}=5.0V	V_{IN} = V_{CC} or V_{SS}		0.01	0.5	μA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or GND			1.0	μA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}			1.0	μA
V_{IL1}	Input Low Level	V_{CC}=1.8V to 5.5V	-0.3		V_{CC}*0.3	V
V_{IH1}	Input High Level	V_{CC}=1.8V to 5.5V	V_{CC}*0.7		V_{CC}+0.3	V
V_{OL2}	Output Low Level V_{CC}=5.0V	I_{OL} = 3.0 mA			0.4	V
V_{OL1}	Output Low Level V_{CC}=1.7V	I_{OL} = 0.15 mA			0.2	V

AC Characteristics

Applicable over recommended operating range from T_A = -40℃ to +85℃, V_{CC} = +1.7V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	1.7V≦V_{CC}<2.5V			2.5V≦V_{CC}≦5.5V			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCL}	Clock Frequency, SCL			400			1000	kHz
T_{LOW}	Clock Pulse Width Low	0.6			0.6			s
T_{HIGH}	Clock Pulse Width High	0.4			0.4			s
T_I	Noise Suppression Time			50			50	ns
T_{AA}	Clock Low to Data Out Valid	0.1		0.55	0.1		0.55	s
T_{BUF}	Time the bus must be free before a new transmission can Start	0.5			0.5			s
$T_{HD.STA}$	Start Hold Time	0.25			0.25			s
$T_{SU.STA}$	Start Setup Time	0.25			0.25			s
$T_{HD.DAT}$	Data In Hold Time	0			0			s
$T_{SU.DAT}$	Data In Setup Time	100			100			ns
T_R	Inputs Rise Time (1)			0.3			0.3	µs
T_F	Inputs Fall Time (1)			0.3			0.3	µs
$T_{SU.STO}$	Stop Setup Time	0.25			0.25			s
T_{DH}	Data Out Hold Time	50			50			ns
T_{WR}	Write Cycle Time		1.9	3		1.9	3	ms
Endurance	5.0V, 25℃, Page Mode(1)	4M						Write Cycles

Notes:

1. This parameter is characterized and is not 100% tested.
2. AC measurement conditions: RL (connects to VCC): 1.3 k
   Input pulse voltages: 0.3 VCC to 0.7 VCC Input rise and fall time: 50 ns
   Input and output timing reference voltages: 0.5 VCC
   The value of RL should be concerned according to the actual loading on the user's system.

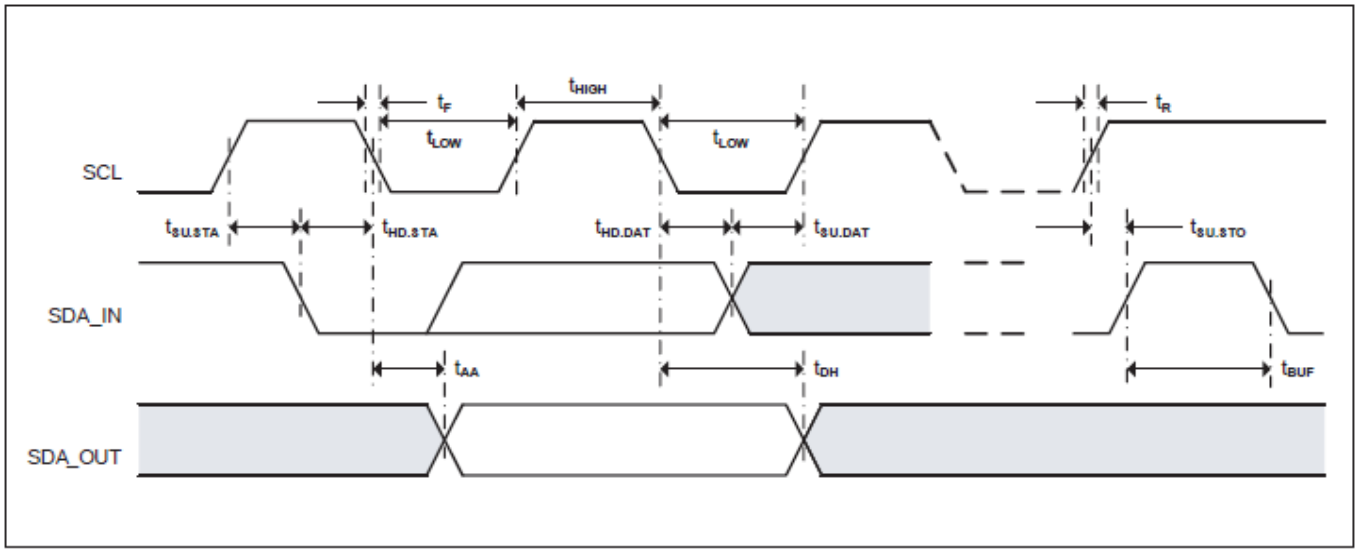


Figure 10 · SCL: Serial Clock, SDA: Serial Data I/O

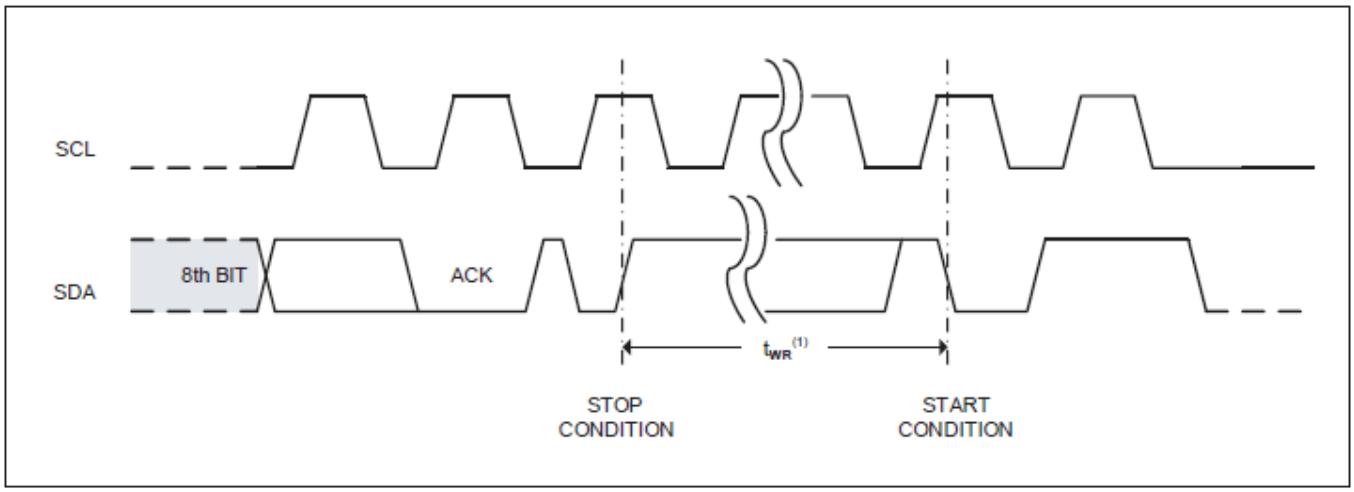
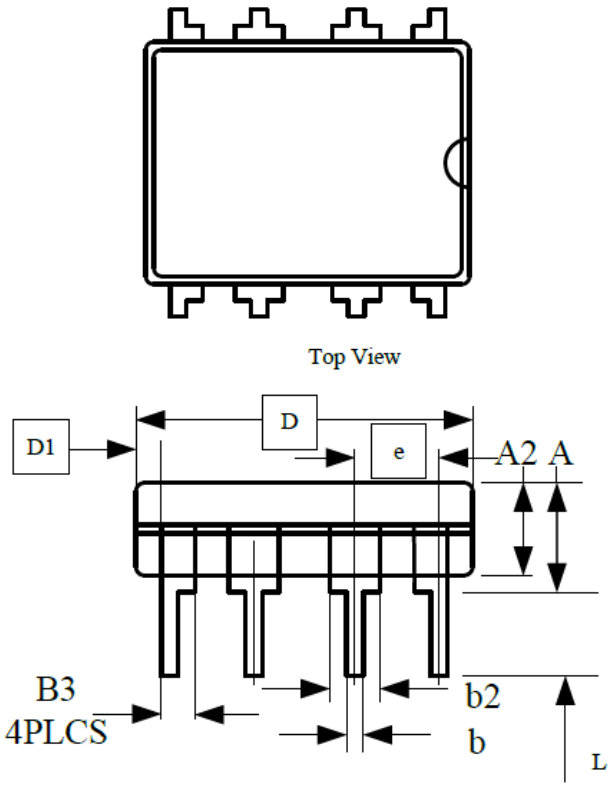


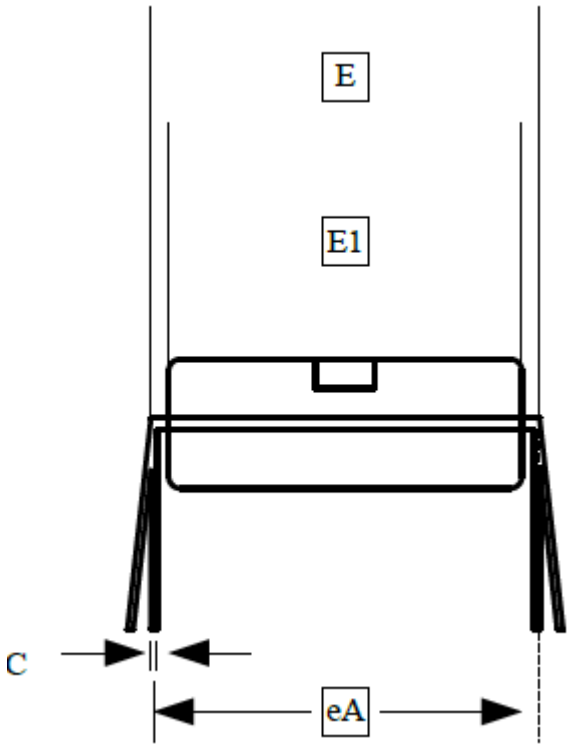
Figure 11 · SCL: Serial Clock, SDA: Serial Data I/O

Note: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Packaging information

DIP-8



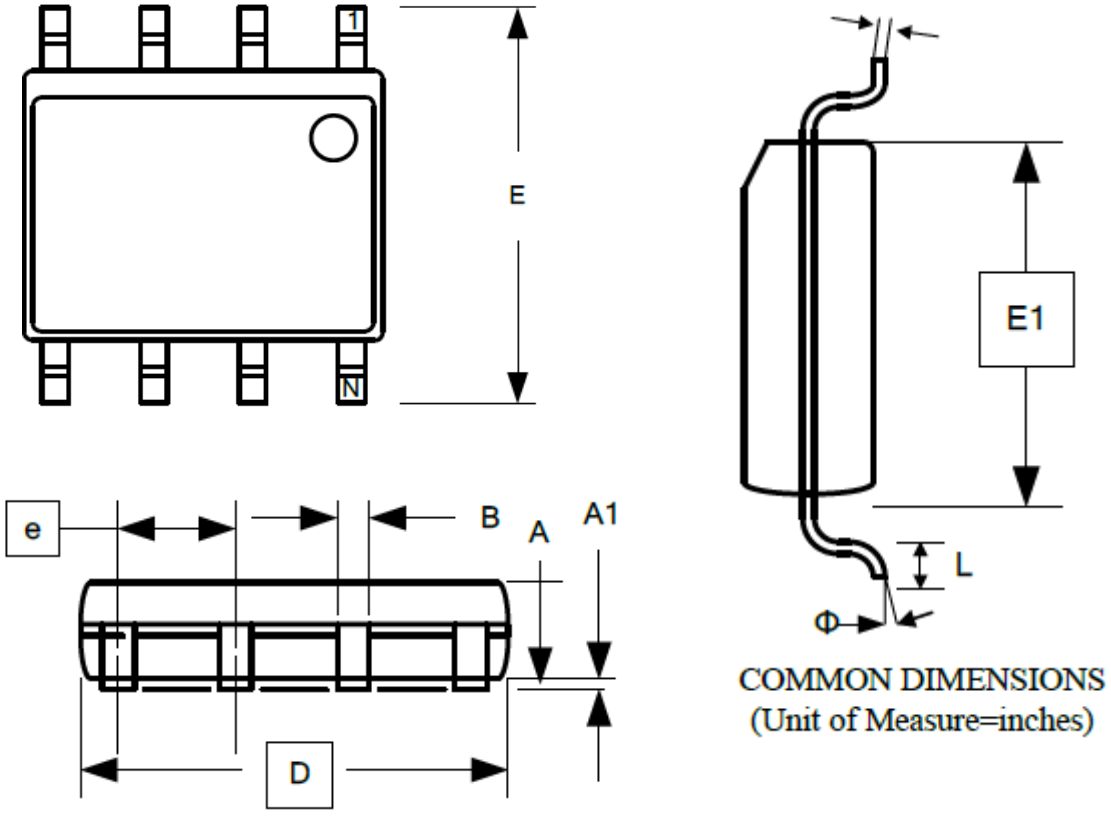


COMMON DIMENSIONS
(Unit of Measure=inches)

SYMBOL	MIN	NOM	MAX	NOTE
A			0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005			3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100BSC			
eA	0.300BSC			4
L	0.115	0.130	0.150	2

Packaging information

SOP-8

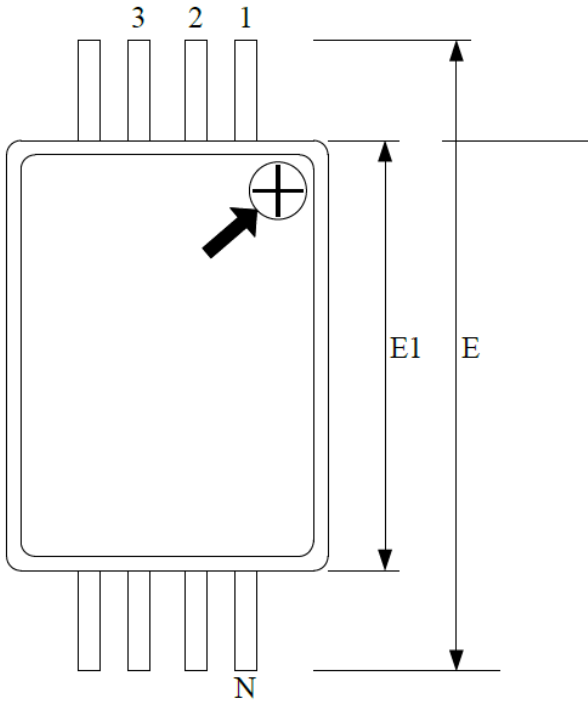


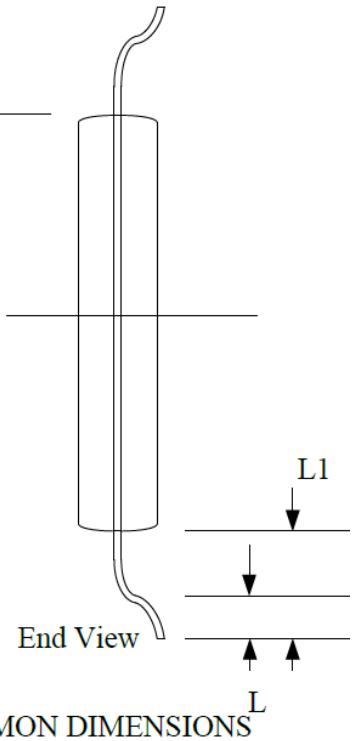
COMMON DIMENSIONS
(Unit of Measure=inches)

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.31		0.51
C	0.17		0.25
D	4.80		5.00
E1	3.81		3.99
E	5.79		6.20
e	1.27BSC		
L	0.40		1.27
Φ	0"		8"

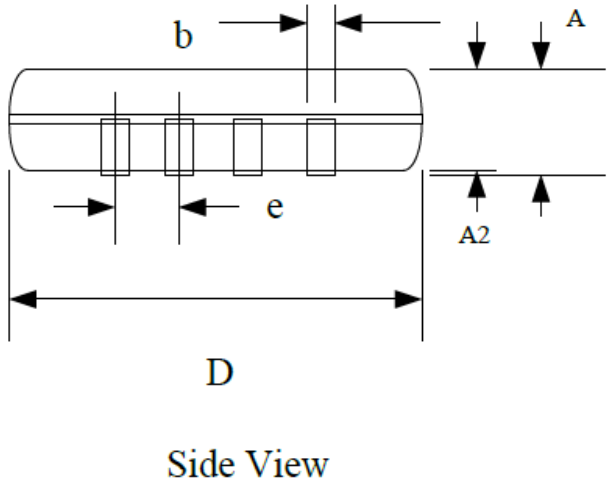
Packaging information

TSSOP-8





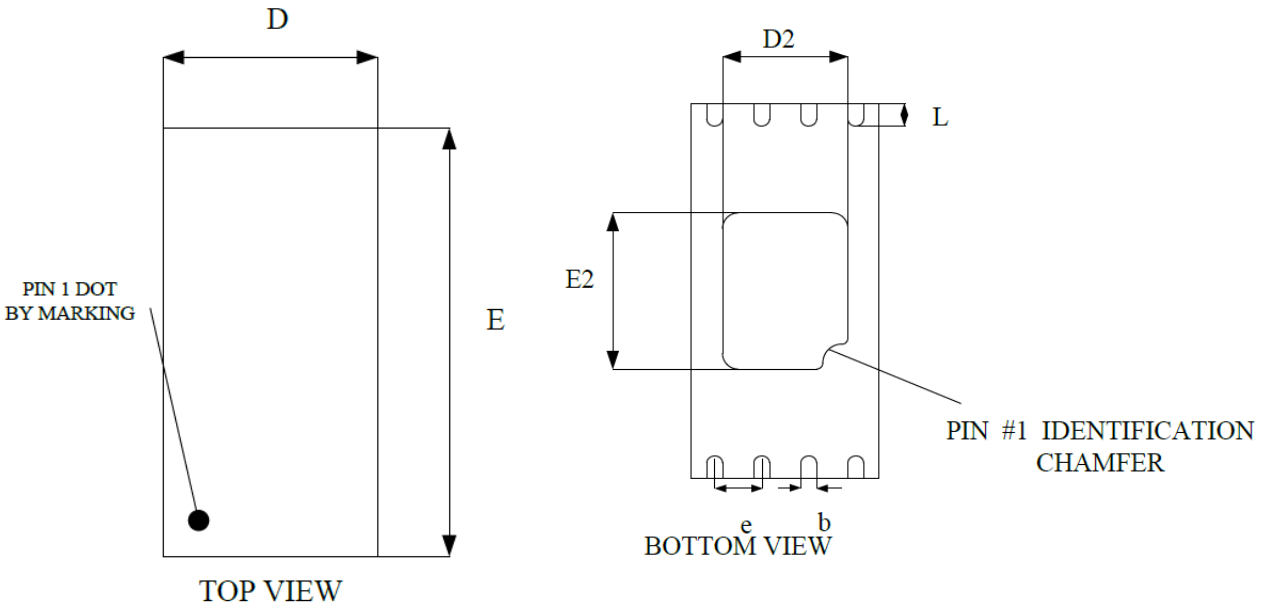
COMMON DIMENSIONS
Unit of Measure=mm

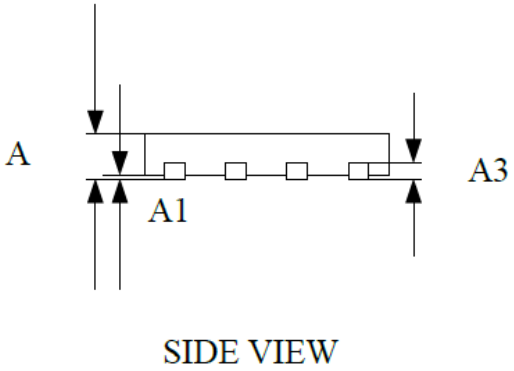


SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2,5
E		6.40BSC		
E1	4.30	4.40	4.50	3,5
A			1.20	
A2	0.80	1.00	1.05	
b	0.19		0.30	4
e		0.65BC		
L	0.45	0.60	0.75	
L1		1.00REF		

Packaging information

USON3*2-8





COMMON DIMENSION(MM)			
PKG	UT:ULTRA THIN		
REF	MIN	NOM	MAX
A	>0.50	0.55	0.60
A1	0.00		0.05
A3	0.15REF		
D	1.95	2.00	2.05
E	2.95	3.00	3.05
b	0.20	0.25	0.30
L	0.20	0.30	0.40
D2	1.25	1.40	1.50
E2	1.15	1.30	1.40
e	0.50BSC		

Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Electronics Co., LTD. As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and shoes failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.